AFFILIATED INSTITUTIONS

ANNA UNIVERSITY, CHENNAI

REGULATIONS - 2013

M.E. VLSI DESIGN

I TO IV SEMESTERS CURRICULA AND SYLLABI (FULL TIME)

SEMESTER I

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1.	MA7157	Applied Mathematics for Electronics Engineers	3	1	0	4
2.	VL7101	VLSI Signal Processing	3	0	0	3
3.	VL7102	VLSI Design Techniques	3	0	0	3
4.	VL7103	Solid State Device Modelling and Simulation	3	0	0	3
5.		Elective I	3	0	0	3
6.		Elective II	3	0	0	3
PRACTICAL						
7.	VL7111	VLSI Design Laboratory I	0	0	3	2
		TOTAL	**18**	**1**	**3**	**21**

SEMESTER II

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1.	AP7201	Analysis and Design of Analog Integrated Circuits	3	0	0	3
2.	VL7201	CAD for VLSI Circuits	3	0	0	3
3.	VL7202	Low Power VLSI Design	3	0	0	3
4.		Elective III	3	0	0	3
5.		Elective IV	3	0	0	3
6.		Elective V	3	0	0	3
PRACTICAL						
7.	VL7211	VLSI Design Laboratory II	0	0	3	2
		TOTAL	**18**	**0**	**3**	**20**

SEMESTER III

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1.	VL7301	Testing of VLSI Circuits	3	0	0	3
2.		Elective VI	3	0	0	3
3.		Elective VII	3	0	0	3
PRACTICAL						
1.	VL7311	Project Work (Phase I)	0	0	12	6
		TOTAL	**9**	**0**	**12**	**15**

SEMESTER IV

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
PRACTICAL						
1.	VL7411	Project Work (Phase II)	0	0	24	12
		TOTAL	**0**	**0**	**24**	**12**

TOTAL NO. OF CREDITS:68

LIST OF ELECTIVES

ELECTIVE I

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
1.	AP7008	DSP Integrated Circuits	3	0	0	3
2.	AP7001	Computer Architecture and Parallel Processing	3	0	0	3
3.	AP7202	ASIC and FPGA Design	3	0	0	3
4.	VL7001	Analog and Mixed Mode VLSI Design	3	0	0	3

ELECTIVE II

5.	VL7002	Security Solutions in VLSI	3	0	0	3
6.	VL7003	Genetic Algorithms and its Applications	3	0	0	3
7.	VL7004	Asynchronous System Design	3	0	0	3

ELECTIVE III

8.	CU7002	MEMS and NEMS	3	0	0	3
9.	VL7005	Physical Design of VLSI Circuits	3	0	0	3
10.	VL7006	Analog VLSI Design	3	0	0	3
11.	VL7007	Process and Device Simulation	3	0	0	3

ELECTIVE IV

12.	VL7008	Design of Semiconductor Memories	3	0	0	3
13.	AP7071	Hardware Software Co-Design	3	0	0	3
14.	CU7001	Real Time Embedded Systems	3	0	0	3
15.	VL7009	Nano Scale Transistors	3	0	0	3

ELECTIVE V

16.	AP7016	System on Chip design	3	0	0	3
17.	CP7023	Reconfigurable Computing	3	0	0	3
18.	VL7010	Submicron VLSI Design	3	0	0	3

ELECTIVE VI

19.	AP7301	Electro Magnetic Interference and Compatibility	3	0	0	3
20.	VL7011	Signal Integrity for High Speed Devices	3	0	0	3
21.	VL7012	Mixed signal IC Test and Measurements	3	0	0	3

ELECTIVE VII

22.	AP7010	Data Converters	3	0	0	3
23.	VL7013	VLSI for Wireless Communication	3	0	0	3
24.	VL7014	IP Based VLSI Design	3	0	0	3
25.	VL7015	Nanoscale Devices and Circuit Design	3	0	0	3

MA7157 APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS L T P C
3 1 0 4

UNIT I FUZZY LOGIC 12
Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers.

UNIT II MATRIX THEORY 12
Some important matrix factorizations – The Cholesky decomposition – QR factorization – Least squares method – Singular value decomposition - Toeplitz matrices and some applications.

UNIT III ONE DIMENSIONAL RANDOM VARIABLES 12
Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Random Variable.

UNIT IV DYNAMIC PROGRAMMING 12
Dynamic programming – Principle of optimality – Forward and backward recursion – Applications of dynamic programming – Problem of dimensionality.

UNIT V QUEUEING MODELS 12
Poisson Process – Markovian queues – Single and Multi-server Models – Little's formula - Machine Interference Model – Steady State analysis – Self Service queue.

L = 45 T=15TOTAL: 60 PERIODS

REFERENCES:

1. George J. Klir and Yuan, B., Fuzzy sets and fuzzy logic, Theory and applications, Prentice Hall of India Pvt. Ltd., 1997.
2. Moon, T.K., Sterling, W.C., Mathematical methods and algorithms for signal processing, Pearson Education, 2000.
3. Richard Johnson, Miller & Freund's Probability and Statistics for Engineers, 7th Edition, Prentice – Hall of India, Private Ltd., New Delhi (2007).
4. Taha, H.A., Operations Research, An introduction, 7th edition, Pearson education editions, Asia, New Delhi, 2002.
5. Donald Gross and Carl M. Harris, Fundamentals of Queuing theory, 2nd edition, John Wiley and Sons, New York (1985).

VL7101 VLSI SIGNAL PROCESSING L T P C
3 0 0 3

OBJECTIVES
- To understand the various VLSI architectures for digital signal processing.
- To know the techniques of critical path and algorithmic strength reduction in the filter structures.
- To study the performance parameters, viz. area, speed and power.

OUTCOMES
- To be able to design architectures for DSP algorithms.
- To be able to optimize design in terms of area, speed and power.
- To be able to incorporate pipeline based architectures in the design.
- To be able to carry out HDL simulation of various DSP algorithms.

UNIT I INTRODUCTION 6
Overview of DSP – FPGA Technology – DSP Technology requirements – Design Implementation.

UNIT II METHODS OF CRITICAL PATH REDUCTION 12

Binary Adders – Binary Multipliers – Multiply-Accumulator (MAC) and sum of product (SOP) – Pipelining and parallel processing – retiming – unfolding – systolic architecture design.

UNIT III ALGORITHMIC STRENGTH REDUCTION METHODS AND RECURSIVE FILTER DESIGN 9

Fast convolution-pipelined and parallel processing of recursive and adaptive filters – fast IIR filters design.

UNIT IV DESIGN OF PIPELINED DIGITAL FILTERS 9

Designing FIR filters – Digital lattice filter structures – bit level arithmetic architecture – redundant arithmetic – scaling and round-off noise.

UNIT V SYNCHRONOUS ASYNCHRONOUS PIPELINING AND PROGRAMMABLE DSP 9

Numeric strength reduction – synchronous – wave and asynchronous pipelines – low power design – programmable DSPs – DSP architectural features/alternatives for high performance and low power.

TOTAL: 45 PERIODS

REFERENCES:

1. Keshab K.Parhi, “VLSI Digital Signal Processing Systems, Design and Implementation”, John Wiley, Indian Reprint, 2007.
2. U. Meyer – Baese, "Digital Signal Processing with Field Programmable Arrays", Springer, Second Edition, Indian Reprint, 2007.
3. S.Y.Kuang, H.J. White house, T. Kailath, “VLSI and Modern Signal Processing”, Prentice Hall, 1995.

VL7102 VLSI DESIGN TECHNIQUES L T P C
3 0 0 3

OBJECTIVES:

- To understand the concepts of MOS transistors operations and their AC , DC characteristics.
- To know the fabrication process of cmos technology and its layout design rules
- To understand the latch up problem in cmos circuits.
- To study the concepts of cmos invertors and their sizing methods
- To know the concepts of power estimation and delay calculations in cmos circuits.

UNIT I MOS TRANSISTOR THEORY 9

NMOS and PMOS transistors, CMOS logic, MOS transistor theory – Introduction, Enhancement mode transistor action, Ideal I-V characteristics, DC transfer characteristics, Threshold voltage-Body effect- Design equations- Second order effects. MOS models and small signal AC characteristics, Simple MOS capacitance Models, Detailed MOS gate capacitance model, Detailed MOS Diffusion capacitance model

UNIT II CMOS TECHNOLOGY AND DESIGN RULE 9

CMOS fabrication and Layout, CMOS technologies, P -Well process, N -Well process, twin -tub process, MOS layers stick diagrams and Layout diagram, Layout design rules, Latch up in CMOS circuits, CMOS process enhancements, Technology – related CAD issues, Fabrication and packaging.

UNIT III INVERTERS AND LOGIC GATES 9

NMOS and CMOS Inverters, Inverter ratio, DC and transient characteristics , switching times, Super buffers, Driving large capacitance loads, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design.

UNIT IV CIRCUIT CHARACTERISATION AND PERFORMANCE ESTIMATION 9

Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining. Charge sharing .Scaling.

UNIT V VLSI SYSTEM COMPONENTS CIRCUITS AND SYSTEM LEVEL PHYSICAL DESIGN 9

Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers. Physical design – Delay modelling ,cross talk, floor planning, power distribution. Clock distribution. Basics of CMOS testing.

TOTAL: 45 PERIODS

REFERENCES

1. Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education ASIA, 2nd edition, 2000.
2. John P.Uyemura “Introduction to VLSI Circuits and Systems”, John Wiley & Sons, Inc., 2002.
3. Eugene D.Fabricius, Introduction to VLSI Design McGraw Hill International Editions, 1990.
4. Pucknell, “Basic VLSI Design”, Prentice Hall of India Publication, 1995.
5. Wayne Wolf “Modern VLSI Design System on chip. Pearson Education, 2002.

VL7103 SOLID STATE DEVICE MODELING AND SIMULATION L T P C
3 0 0 3

OBJECTIVE:

To acquaint the students with fundamentals of building device and circuit simulators, and efficient use of simulators.

UNIT I MOSFET DEVICE PHYSICS 9

MOSFET capacitor, Basic operation, Basic modeling,Advanced MOSFET modeling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, Highfrequency behavior of MOS transistor and A.C small signal modeling, model parameter
extraction, modeling parasitic BJT, Resistors, Capacitors, Inductors.

UNIT II DEVICE MODELLING 9

Prime importance of circuit and device simulations in VLSI; Nodal, mesh, modified nodal and hybrid analysis equations. Solution of network equations: Sparse matrix techniques, solution of nonlinear networks through Newton-Raphson technique, convergence and stability.

UNIT III MULTISTEP METHODS 9

Solution of stiff systems of equations, adaptation of multistep methods to the solution of electrical networks, general purpose circuit simulators.

UNIT IV MATHEMATICAL TECHNIQUES FOR DEVICE SIMULATIONS 9

Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, hydrodynamic equations, trap rate, finite difference solutions to these equations in 1D and 2D space, grid generation.

UNIT V SIMULATION OF DEVICES 9

Computation of characteristics of simple devices like p-n junction, MOS capacitor and MOSFET; Small-signal analysis.

TOTAL :45 PERIODS

REFERENCES

1. Arora, N., “MOSFET Models for VLSI Circuit Simulation”, Springer-Verlag, 1993
2. Selberherr, S., “Analysis and Simulation of Semiconductor Devices”, Springer-Verlag., 1984
3. Fjeldly, T., Yetterdal, T. and Shur, M., “Introduction to Device Modeling and Circuit Simulation”, Wiley-Interscience., 1997
4. Grasser, T., “Advanced Device Modeling and Simulation”, World Scientific Publishing Company., 2003
5. Chua, L.O. and Lin, P.M., “Computer-Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques”, Prentice-Hall., 1975
6. Trond Ytterdal, Yuhua Cheng and Tor A. FjeldlyWayne Wolf, “Device Modeling for Analog and RF CMOS Circuit Design”, John Wiley & Sons Ltd.

VL7111 VLSI DESIGN LABORATORY I L T P C
0 0 3 2

1. Design of NMOS and CMOS Inverters - DC and transient characteristics and switching times
2. Estimation of Resistance, Capacitance and Inductance
3. Design of Multiplexers, Decoders and comparators
4. Analytical Modeling and simulation of I-V characteristics of a p channel/n channel MOSFET using Newton Raphson method
5. Analytical Modeling and simulation of potential distribution/field of the MOSFET using finite difference method
6. Modeling and analysis of MOS capacitor - Small signal Analysis
7. Simulation of Schrodinger equation based device modeling
8. Modeling and Simulation of NMOS and CMOS circuits using Spice
9. Design of Designing FIR filters using FPGA

TOTAL:45 PERIODS

AP7201 ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS L T P C
3 0 0 3

OBJECTIVES:

- To design the single stage amplifiers using pmos and nmos driver circuits with different loads.
- To analyse high frequency concepts of single stage amplifiers and noise characteristics associated with differential amplifiers.
- To study the different types of current mirrors and To know the concepts of voltage and current reference circuits.

UNIT I SINGLE STAGE AMPLIFIERS 9

Common source stage, Source follower, Common gate stage, Cascode stage, Single ended and differential operation, Basic differential pair, Differential pair with MOS loads

UNIT II FREQUENCY RESPONSE AND NOISE ANALYSIS 9

Miller effect ,Association of poles with nodes, frequency response of common source stage, Source followers, Common gate stage, Cascode stage, Differential pair, Statistical characteristics of noise, noise in single stage amplifiers, noise in differential amplifiers.

UNIT III OPERATIONAL AMPLIFIERS 9

Concept of negative feedback, Effect of loading in feedback networks, operational amplifier performance parameters, One-stage Op Amps, Two-stage Op Amps, Input range limitations, Gain boosting, slew rate, power supply rejection, noise in Op Amps.

UNIT IV STABILITY AND FREQUENCY COMPENSATION 9

General considerations, Multipole systems, Phase Margin, Frequency Compensation, Compensation of two stage Op Amps, Slewing in two stage Op Amps, Other compensation techniques.

UNIT V BIASING CIRCUITS 9

Basic current mirrors, cascode current mirrors, active current mirrors, voltage references, supply independent biasing, temperature independent references, PTAT current generation, Constant-Gm Biasing.

TOTAL: 45 PERIODS

REFERENCES:

1. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, Analysis and Design of Analog Integrated Circuits, 5th Edition, Wiley, 2009.
2. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Tata McGraw Hill, 2001
3. Willey M.C. Sansen, “Analog design essentials”, Springer, 2006.
4. Grebene, “Bipolar and MOS Analog Integrated circuit design”, John Wiley & sons, Inc., 2003.
5. Phillip E.Allen, Douglas R.Holberg, “CMOS Analog Circuit Design”, Second edition, Oxford University Press, 2002

VL7201 CAD FOR VLSI CIRCUITS L T P C
3 0 0 3

OBJECTIVES:

- To study various physical design methods in VLSI.
- To understand the concepts behind the VLSI design rules and routing techniques.
- To use the simulation techniques at various levels in VLSI design flow,
- To understand the concepts of various algorithms used for floor planning and routing techniques.

UNIT I VLSI DESIGN METHODOLOGIES 9

Introduction to VLSI Design methodologies - Review of Data structures and algorithms - Review of VLSI Design automation tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization.

UNIT II DESIGN RULES 9

Layout Compaction - Design rules - problem formulation - algorithms for constraint graph compaction - placement and partitioning - Circuit representation - Placement algorithms – partitioning

UNIT III FLOOR PLANNING 9

Floor planning concepts - shape functions and floorplan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing.

UNIT IV SIMULATION 9

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation- Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

UNIT V MODELLING AND SYNTHESIS **9**

High level Synthesis - Hardware models - Internal representation - Allocation - assignment and scheduling - Simple scheduling algorithm - Assignment problem - High level transformations.

TOTAL: 45 PERIODS

REFERENCES:

1. S.H. Gerez, "Algorithms for VLSI Design Automation", John Wiley & Sons, 2002.
2. N.A. Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwer Academic Publishers, 2002.
3. Sadiq M. Sait, Habib Youssef, "VLSI Physical Design automation: Theory and Practice", World scientific 1999.
4. Steven M.Rubin, "Computer Aids for VLSI Design", Addison Wesley Publishing 1987.

VL7202 LOW POWER VLSI DESIGN **L T P C**
3 0 0 3

OBJECTIVES:

- To know the sources of power consumption in cmos circuits
- To understand the various power reduction techniques and the power estimation methods.
- To study the design concepts of low power circuits.

UNIT I POWER DISSIPATION IN **9**

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Basic principle of low power design.

UNIT II POWER OPTIMIZATION **9**

Logic level power optimization – Circuit level low power design – circuit techniques for reducing power consumption in adders and multipliers.

UNIT III DESIGN OF LOW POWER CIRCUITS **9**

Computer arithmetic techniques for low power system – reducing power consumption in memories – low power clock, Inter connect and layout design – Advanced techniques –Special techniques.

UNIT IV POWER ESTIMATION **9**

Power Estimation technique – logic power estimation – Simulation power analysis – Probabilistic power analysis.

UNIT V SYNTHESIS AND SOFTWARE DESIGN **9**

Synthesis for low power – Behavioral level transform – software design for low power.

TOTAL: 45 PERIODS

REFERENCES:

1. Kaushik Roy and S.C.Prasad, "Low power CMOS VLSI circuit design", Wiley, 2000.
2. Dimitrios Soudris, Christians Pignet, Costas Goutis, "Designing CMOS Circuits for Low Power", Kluwer, 2002.
3. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley 1999.
4. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer,1995.
5. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.
6. Abdelatif Belaouar, Mohamed.I.Elmasry, "Low power digital VLSI design", Kluwer, 1995.
7. James B.Kulo, Shih-Chia Lin, "Low voltage SOI CMOS VLSI devices and Circuits", John Wiley and sons, inc. 2001.
8. Steven M.Rubin, "Computer Aids for VLSI Design", Addison Wesley Publishing.

VL7211 VLSI DESIGN LABORATORY II L T P C
0 0 3 2

1. Design and simulate frequency response and noise analysis of any Source followers
2. Design and simulate Design and simulate operational amplifier performance parameters - One-stage Op Amps, Two-stage Op Amps
3. Design and simulate cascode current mirrors and active current mirrors
4. Design of various routing - local routing, Area routing, channel routing and global routing
5. Design and Simulation of Gate-level modeling
6. Design and Simulation of Switch-level modeling
7. Modeling and synthesis of simple scheduling algorithm
8. Design and implement reducing power consumption in memories
9. Design and simulate Power Estimation

TOTAL: 45 PERIODS

VL7301 TESTING OF VLSI CIRCUITS L T P C
3 0 0 3

OBJECTIVES:

- To know the various types of faults and also to study about fault detection, dominance
- To know the concepts of the test generation methods-DFT-BIST.
- To understand the fault diagnosis methods.

UNIT I TESTING AND FAULT MODELLING 9

Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models – Fault detection – Fault Location – Fault dominance – Logic simulation – Types of simulation – Delay models – Gate Level Event – driven simulation.

UNIT II TEST GENERATION 9

Test generation for combinational logic circuits – Testable combinational logic circuit design – Test generation for sequential circuits – design of testable sequential circuits.

UNIT III DESIGN FOR TESTABILITY 9

Design for Testability – Ad-hoc design – generic scan based design – classical scan based design – system level DFT approaches.

UNIT IV SELF – TEST AND TEST ALGORITHMS 9

Built-In self Test – test pattern generation for BIST – Circular BIST – BIST Architectures – Testable Memory Design – Test Algorithms – Test generation for Embedded RAMs.

UNIT V FAULT DIAGNOSIS 9

Logical Level Diagnosis – Diagnosis by UUT reduction – Fault Diagnosis for Combinational Circuits – Self-checking design – System Level Diagnosis.

TOTAL: 45 PERIODS

REFERENCES:

1. M.Abramovici, M.A.Breuer and A.D. Friedman, “Digital systems and Testable Design”, Jaico Publishing House, 2002.
2. P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002.
3. M.L.Bushnell and V.D.Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwer Academic Publishers, 2002.
4. A.L.Crouch, “Design Test for Digital IC’s and Embedded Core Systems”, Prentice Hall International, 2002.

AP7008 DSP INTEGRATED CIRCUITS L T P C
3 0 0 3

OBJECTIVES:

1. To study the procedural flow of system design in DSP and Integrated circuit.
2. To analyse the frequency response and transfer function of DSP systems.
3. To compare and study the performance of various transforms for signal processing.
4. To design FIR and IIR filters for the given specifications.
5. To study the architectures for DSP system.
6. To study the design layout for VLSI circuits.

UNIT I DSP INTEGARTED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES 9

Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic, VLSI process technologies, Trends in CMOS technologies.

UNIT II DIGITAL SIGNAL PROCESSING 9

Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal-processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms.

UNIT III DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects -Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT IV DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES 9

DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.

UNIT V ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN 9

Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies. Cordic algorithm.

TOTAL: 45 PERIODS

REFERENCES:

1. Lars Wanhammer, "DSP Integrated Circuits", 1999 Academic press, New York
2. A.V.Oppenheim et.al, "Discrete-time Signal Processing", Pearson Education, 2000.
3. Emmanuel C. Ifeachor, Barrie W. Jervis, "Digital signal processing – A practical approach", Second Edition, Pearson Education, Asia.
4. Keshab K.Parhi, "VLSI Digital Signal Processing Systems design and Implementation", John Wiley & Sons, 1999.

AP7001 COMPUTER ARCHITECTURE AND PARALLEL PROCESSING L T P C
3 0 0 3

OBJECTIVES:

- To understand the difference between the pipeline and parallel concepts.
- To study the various types of architectures and the importance of scalable architectures.
- To study the various memories and optimization of memory.

UNIT I COMPUTER DESIGN AND PERFORMANCE MEASURES 9

Fundamentals of Computer Design – Parallel and Scalable Architectures – Multiprocessors – Multivector and SIMD architectures – Multithreaded architectures – Data-flow architectures - Performance Measures

UNIT II PARALLEL PROCESSING, PIPELINING AND ILP 9

Instruction Level Parallelism and Its Exploitation - Concepts and Challenges - Overcoming Data Hazards with Dynamic Scheduling – Dynamic Branch Prediction - Speculation - Multiple Issue Processors - Performance and Efficiency in Advanced Multiple Issue Processors

UNIT III MEMORY HIERARCHY DESIGN 9

Memory Hierarchy - Memory Technology and Optimizations – Cache memory – Optimizations of Cache Performance – Memory Protection and Virtual Memory - Design of Memory Hierarchies

UNIT IV MULTIPROCESSORS 9

Symmetric and distributed shared memory architectures – Cache coherence issues - Performance Issues – Synchronization issues – Models of Memory Consistency - Interconnection networks – Buses, crossbar and multi-stage switches.

UNIT V MULTI-CORE ARCHITECTURES 9

Software and hardware multithreading – SMT and CMP architectures – Design issues – Case studies – Intel Multi-core architecture – SUN CMP architecture – IBM cell architecture - hp architecture.

TOTAL:45 PERIODS

REFERENCES:

1. Kai Hwang, "Advanced Computer Architecture", McGraw Hill International, 2001.
2. John L. Hennessey and David A. Patterson, “Computer Architecture – A quantitative approach”, Morgan Kaufmann / Elsevier, 4th. edition, 2007.
3. William Stallings, “Computer Organization and Architecture – Designing for Performance”, Pearson Education, Seventh Edition, 2006.
4. John P. Hayes, “Computer Architecture and Organization”, McGraw Hill
5. David E. Culler, Jaswinder Pal Singh, “Parallel Computing Architecture: A hardware/ software approach”, Morgan Kaufmann / Elsevier, 1997.
6. Dimitrios Soudris, Axel Jantsch, "Scalable Multi-core Architectures: Design Methodologies and Tools", Springer, 2012
7. John P. Shen, “Modern processor design. Fundamentals of super scalar processors”, Tata McGraw Hill 2003.

AP7202 ASIC AND FPGA DESIGN L T P C
3 0 0 3

OBJECTIVES:

- To study the design flow of different types of ASIC.
- To familiarize the different types of programming technologies and logic devices.
- To learn the architecture of different types of FPGA.
- To gain knowledge about partitioning, floor planning, placement and routing including circuit extraction of ASIC
- To analyse the synthesis, Simulation and testing of systems.
- To understand the design issues of SOC.
- To know about different high performance algorithms and its applications in ASICs.

UNIT I OVERVIEW OF ASIC AND PLD 9

Types of ASICs - Design flow – CAD tools used in ASIC Design – Programming Technologies: Antifuse – static RAM – EPROM and EEPROM technology, Programmable Logic Devices: ROMs and EPROMs – PLA –PAL. Gate Arrays – CPLDs and FPGAs

UNIT II ASIC PHYSICAL DESIGN 9

System partition -partitioning - partitioning methods – interconnect delay models and measurement of delay - floor planning - placement – Routing: global routing - detailed routing - special routing - circuit extraction - DRC

UNIT III LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation. Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

UNIT IV FPGA 9

Field Programmable gate arrays- Logic blocks, routing architecture, Design flow technology - mapping for FPGAs, Xilinx XC4000 - ALTERA's FLEX 8000/10000, ACTEL's ACT-1,2,3 and their speed performance

Case studies: Altera MAX 5000 and 7000 - Altera MAX 9000 – Spartan II and Virtex II FPGAs - Apex and Cyclone FPGAs

UNIT V SOC DESIGN 9

Design Methodologies – Processes and Flows - Embedded software development for SOC – Techniques for SOC Testing – Configurable SOC – Hardware / Software co design Case studies: Digital camera, Bluetooth radio / modem, SDRAM and USB

TOTAL: 45 PERIODS

REFERENCES:

1. M.J.S .Smith, "Application Specific Integrated Circuits, Addison -Wesley Longman Inc., 1997
2. S. Trimberger, Field Programmable Gate Array Technology, Edr, Kluwer Academic Publications, 1994.
3. John V.Oldfield, Richard C Dore, Field Programmable Gate Arrays, Wiley Publications 1995.
4. P.K.Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, Prentice Hall, 1994.
5. Parag.K.Lala, Digital System Design using Programmable Logic Devices , BSP, 2003.
6. S. Brown, R. Francis, J. Rose, Z. Vransic, Field Programmable Gate Array, Kluwer Pubin, 1992.
7. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley & Sons, New York, 1995.
8. Farzad Nekoogar and Faranak Nekoogar, From ASICs to SOCs: A Practical Approach, Prentice Hall PTR, 2003.
9. Wayne Wolf, FPGA-Based System Design, Prentice Hall PTR, 2004.
10. R. Rajsuman, System-on-a-Chip Design and Test. Santa Clara, CA: Artech House Publishers, 2000.
11. F. Nekoogar. Timing Verification of Application-Specific Integrated Circuits (ASICs).Prentice Hall PTR, 1999.

VL7001 ANALOG AND MIXED MODE VLSI DESIGN **L T P C**
3 0 0 3

OBJECTIVES:

- To study the concepts of MOS large signal model and small signal model
- To understand the concepts of D/A conversion methods and their architectures.
- To design filters for ADC.
- To study about the switched capacitor circuits.

UNIT I INTRODUCTION AND BASIC MOS DEVICES **9**

Challenges in analog design-Mixed signal layout issues- MOS FET structures and characteristics-large signal model – small signal model- single stage Amplifier-Source follower- Common gate stage – Cascode Stage

UNIT II SIBMICRON CIRCUIT DESIGN **9**

Submicron CMOS process flow, Capacitors and resistors, Current mirrors, Digital Circuit Design, Delay Elements – Adders- OP Amp parameters and Design

UNIT III DATA CONVERTERS **9**

Characteristics of Sample and Hold- Digital to Analog Converters- architecture-Differential Non linearity-Integral Non linearity- Voltage Scaling-Cyclic DAC-Pipeline DAC-Analog to Digital Converters- architecture – Flash ADC-Pipeline ADC-Differential Non linearity-Integral Non linearity

UNIT IV SNR IN DATA CONVERTERS **9**

Overview of SNR of Data Converters- Clock Jitters- Improving Using Averaging – Decimating Filters for ADC- Band pass and High Pass Sinc Filters- Interpolating Filters for DAC

UNIT V SWITCHED CAPACITOR CIRCUITS **9**

Resistors, First order low pass Circuit, Switched capacitor Amplifier, Switched Capacitor Integrator

TOTAL: 45 PERIODS

REFERENCES:

1. Vineetha P.Gejji Analog and Mixed Mode Design **-** Prentice Hall, 1st Edition , 2011
2. JeyaGowri Analog and Mixed Mode Design- Sapna publishing House 2011.

VL7002 SECURITY SOLUTIONS IN VLSI **L T P C**
3 0 0 3

OBJECTIVES:

1. To study the different kinds of threats to information security.
2. To know the various techniques for data encryption.
3. To formulate case study based on VLSI for security threats.
4. To design and implement the various cryptography algorithms in VLSI.

UNIT I BASIC CONCEPTS **9**

Information system reviewed, LAN, MAN, WAN, Information flow, Security mechanism in OS,,Targets: Hardware, Software, Data communication procedures. Threats to Security: Physical security, Biometric systems, monitoring controls, Data security, systems, security, Computer System security, communication security.

UNIT II ENCRYPTION TECHNIQUES **9**

Conventional techniques, Modern techniques, DES, DES chaining+, Triple DES, RSA algorithm, Key management. Message Authentication and Hash Algorithm: Authentication requirements and functions secure Hash Algorithm, NDS message digest algorithm, digital signatures, Directory authentication service.

UNIT III FIREWALLS AND CYBER LAWS **9**

Firewalls, Design Principles, Trusted systems, IT act and cyber laws, Virtual private network.

UNIT IV FUTURE THREATS TO NETWORK: **9**

Recent attacks on networks, VLSI Based Case study

UNIT V CRYPTO CHIP DESIGN: **9**

VLSI Implementation of AES algorithm. Implementation of DES, IDEA AES algorithm, Development of digital signature chip using RSA algorithm.

REFERENCES:

1. William Stalling "Cryptography and Network Security" Pearson Education, 2005
2. Charels P. Pfleeger "Security in Computing" Prentice Hall, 2006
3. Jeff Crume "Inside Internet Security" Addison Wesley, 2000.

VL7003 GENETIC ALGORITHMS AND ITS APPLICATIONS **L T P C**
3 0 0 3

UNIT I **9**

Introduction, GA Technology-Steady State Algorithm-Fitness Scaling-Inversion

UNIT II **9**

GA for VLSI Design, Layout and Test automation-partitioning- automatic placement, routing technology, Mapping for FPGA -Automatic test generation-Partitioning algorithm Taxonomy - Multiway Partitioning

UNIT III **9**

Hybrid genetic – genetic encoding-local improvement-WDFR-Comparison of Cas-Standard cell placement-GASP algorithm-unified algorithm.

UNIT IV **9**

Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures.

UNIT V **9**

Power estimation-application of GA-Standard cell placement-GA for ATG-problem encoding- fitness function-GA vs Conventional algorithm.

TOTAL: 45 PERIODS

REFERENCES:

1. Pinaki Mazumder,E.MRudnick,"Genetic Algorithm for VLSI Design,Layout and test Automation", Prentice Hall,1998.
2. Randy L. Haupt, Sue Ellen Haupt, "Practical Genetic Algorithms" Wiley – Interscience, 1977.
3. Ricardo Sal Zebulum, Macro Aurelio Pacheco, Marley Maria B.R. Vellasco, Marley Maria Bernard Vellasco "Evolution Electronics: Automatic Design of electronic Circuits and Systems Genetic Algorithms", CRC press, 1st Edition Dec 2001.
4. John R.Koza, Forrest H.Bennett III, David Andre , Morgan Kufmann, "Genetic Programming Automatic programming and Automatic Circuit Synthesis", 1st Edition , May 1999.

VL7004 ASYNCHRONOUS SYSTEM DESIGN L T P C
3 0 0 3

OBJECTIVES:

1. To study the basic concepts of handshake circuits for asynchronous architecture.
2. To understand and analyse the performance of handshake circuits.
3. To synthesize and design control circuits for asynchronous system.
4. To familiarize VHDL and the Balsa language for asynchronous design.

UNIT I FUNDAMENTALS 9

Handshake protocols, Muller C-element, Muller pipeline, Circuit implementation styles, theory. Static data-flow structures: Pipelines and rings, Building blocks, examples

UNIT II PERFORMANCE 9

A quantitative view of performance, quantifying performance, Dependency graphic analysis. Handshake circuit implementation: Fork, join, and merge, Functional blocks, mutual exclusion, arbitration and metastability.

UNIT III SPEED-INDEPENDENT CONTROL CIRCUITS 9

Signal Transition graphs, Basic Synthesis Procedure, Implementation using state-holding gates, Summary of the synthesis Process, Design examples using Petrify. Advanced 4-phase bundled data protocols and circuits: Channels and protocols, Static type checking, More advanced latch control circuits.

UNIT IV HIGH-LEVEL LANGUAGES AND TOOLS 9

Concurrency and message passing in CSP, Tangram program examples, Tangram syntax-directed compilation, Martin's translation process, Using VHDL for Asynchronous Design. An Introduction to Balsa: Basic concepts, Tool set and design flow, Ancillary Balsa Tools

UNIT V THE BALSA LANGUAGE 9

Data types, Control flow and commands, Binary/Unary operators, Program structure. Building library Components: Parameterized descriptions, Recursive definitions. A simple DMA controller: Global Registers, Channel Registers, DMA control structure, The Balsa description.Principles of Asynchronous Circuit Design - Jens Sparso, Steve Furber, Kluver AcademicPublishers.

TOTAL:45 PERIODS

TEXT BOOKS:

1. Asynchronous Circuit Design- Chris. J. Myers, John Wiley & Sons, 2001.
2. Handshake Circuits An Asynchronous architecture for VLSI programming – Kees Van Berkel Cambridge University Press, 2004

REFERENCE:

1. Principles of Asynchronous Circuit Design-Jens Sparso, Steve Furber, Kluver Academic Publishers, 2001.

CU7002 MEMS AND NEMS L T P C
3 0 0 3

OBJECTIVES:

- To introducing the concepts of micro electromechanical devices.
- To know the fabrication process of Microsystems.
- To know the design concepts of micro sensors and micro actuators.
- To introducing concepts of quantum mechanics and nano systems.

UNIT I OVERVIEW AND INTRODUCTION 9

New trends in Engineering and Science: Micro and Nanoscale systems Introduction to Design of MEMS and NEMS, Overview of Nano and Microelectromechanical Systems, Applications of Micro and Nanoelectromechanical systems, Microelectromechanical systems, devices and structures Definitions, Materials for MEMS: Silicon, silicon compounds, polymers, metals

UNIT II MEMS FABRICATION TECHNOLOGIES 9

Microsystem fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching; Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect-Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials

UNIT III MICRO SENSORS 9

MEMS Sensors: Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo Resistive Pressure sensors- engineering mechanics behind these Microsensors. Case study: Piezo-resistive pressure sensor

UNIT IV MICRO ACTUATORS 9

Design of Actuators: Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces (Parallel plate, Torsion bar, Comb drive actuators), Micromechanical Motors and pumps. Case study: Comb drive actuators

UNIT V NANOSYSTEMS AND QUANTUM MECHANICS 9

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Shrodinger Equation and Wavefunction Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits

TOTAL:45 PERIODS

REFERENCES:

1. Marc Madou, “Fundamentals of Microfabrication”, CRC press 1997.
2. Stephen D. Senturia,” Micro system Design”, Kluwer Academic Publishers,2001
3. Tai Ran Hsu ,”MEMS and Microsystems Design and Manufacture” ,Tata Mcraw Hill, 2002.
4. Chang Liu, “Foundations of MEMS”, Pearson education India limited, 2006,
5. Sergey Edward Lyshevski, “MEMS and NEMS: Systems, Devices, and Structures” CRC Press, 2002

VL7005 PHYSICAL DESIGN OF VLSI CIRCUITS L T P C
3 0 0 3

OBJECTIVE:

To introduce the physical design concepts such as routing, placement, partitioning and packaging and to study the performance of circuits layout designs, compaction techniques.

UNIT I INTRODUCTION TO VLSI TECHNOLOGY 9

Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates, field programmable gate array(FPGA)-layout methodologies Packaging-Computational Complexity-Algorithmic Paradigms.

UNIT II PLACEMENT USING TOP-DOWN APPROACH 9

Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic Ratio cut-partition with capacity and i/o constrants. Floor planning: Rectangular dual floor planning-hierarchial approach- simulated annealing- Floor plan sizing Placement: Cost function- force directed method- placement by simulated annealing partitioning placement- module placement on a resistive network – regular placement linear placement. 13

UNIT III ROUTING USING TOP DOWN APPROACH 9

Fundamentals: Maze Running- line searching- Steiner trees Global Routing: Sequential Approaches - hierarchial approaches - multi commodity flow based techniques - Randomised Routing- One Step approach - Integer Linear Programming Detailed Routing: Channel Routing - Switch box routing. Routing in FPGA: Array based FPGA- Row based FPGAs

UNIT IV PERFORMANCE ISSUES IN CIRCUIT LAYOUT 9

Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing – Driven Placement: Zero Stack Algorithm- Weight based placement- Linear Programming Approach Timing riving Routing: Delay Minimization- Click Skew Problem- Buffered Clock Trees. Minimization: constrained via Minimization unconstrained via Minimization- Other issues in minimization

UNIT V SINGLE LAYER ROUTING, CELL GENERATION AND COMPACTION 9

Planar subset problem(PSP)- Single Layer Global Routing- Single Layer detailed Routing- Wire length and bend minimization technique – Over The Cell (OTC) Routing Multiple chip modules(MCM)- programmable Logic Arrays- Transistor chaining- Wein Burger Arrays- Gate matrix layout- 1D compaction- 2D compaction.

TOTAL: 45 PERIODS

REFERENCES:

1. Sarafzadeh, C.K. Wong, “An Introduction to VLSI Physical Design”, McGraw Hill International Edition 1995
2. Preas M. Lorenzatti, “ Physical Design and Automation of VLSI systems”, The Benjamin Cummins Publishers, 1998.

VL7006 ANALOG VLSI DESIGN L T P C
3 0 0 3

OBJECTIVE:

To study the concepts of CMOS and BICMOS analog circuits. To understand the concepts of A/Dconvertors and analog integrated sensors. To understand the testing concepts in analog VLSI circuits and its statistical modelling.

UNIT I BASIC CMOS CIRCUIT TECHNIQUES, CONTINUOUS TIME AND LOW-VOLTAGE SIGNAL PROCESSING 9

Mixed-Signal VLSI Chips - Basic CMOS Circuits – Basic Gain Stage - Gain Boosting Techniques – Super MOS Transistor-Primitive Analog Cells-Linear Voltage-Current Converters -MOS Multipliers and Resistors-CMOS, Bipolar and Low-Voltage Bi CMOS Op- Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.

UNIT II BASIC BICMOS CIRCUIT TECHNIQUES, CURRENT -MODE SIGNAL PROCESSING AND NEURAL INFORMATION PROCESSING 9

Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks - Floating - Gate, Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-Contrast Sensitive Silicon Retina.

UNIT III SAMPLED-DATA ANALOG FILTERS, OVER SAMPLED A/D CONVERTERS AND ANALOG INTEGRATED SENSORS 9

First-order and Second SC Circuits-Bilinear Transformation - Cascade Design-Switched-Capacitor Ladder Filter-Synthesis of Switched-Current Filter- Nyquist rate A/D Converters-Modulators for Over sampled A/D Conversion-First and Second Order and Multibit Sigma-Delta Modulators-Interpolative Modulators –Cascaded Architecture-Decimation Filters-mechanical, Thermal, Humidity and Magnetic Sensors-Sensor Interfaces.

UNIT IV DESIGN FOR TESTABILITY AND ANALOG VLSI INTERCONNECTS 9

Fault modelling and Simulation - Testability-Analysis Technique-Ad Hoc Methods and General Guidelines-Scan Techniques-Boundary Scan-Built-in Self Test-Analog Test Buses-Design for Electron -Beam Testablity-Physics of Interconnects in VLSI-Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping Analog Circuits.

UNIT V STATISTICAL MODELING AND SIMULATION, ANALOG COMPUTER- AIDED DESIGN AND ANALOG AND MIXED ANALOG-DIGITAL LAYOUT 9

Review of Statistical Concepts - Statistical Device Modeling- Statistical Circuit Simulation-Automation Analog Circuit Design-automatic Analog Layout-CMOS Transistor Layout-Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog -Digital Layout.

TOTAL: 45 PERIODS

REFERENCES:

1. Mohammed Ismail, Terri Fief, “Analog VLSI signal and Information Processing ", McGraw- Hill International Editons, 1994.
2. Malcom R.Haskard, Lan C.May, “Analog VLSI Design - NMOS and CMOS", Prentice Hall, 1998.
3. Randall L Geiger, Phillip E. Allen, " Noel K.Strader, VLSI Design Techniques for Analog and Digital Circuits ", Mc Graw Hill International Company, 1990.
4. Jose E.France, Yannis Tsividis, “Design of Analog-Digital VLSI Circuits for Telecommunication and signal Processing ", Prentice Hall, 1994

VL7007 PROCESS AND DEVICE SIMULATION L T P C
3 0 0 3

OBJECTIVE:

To study and understand the CAD for VLSI technogies and for device simulation.

UNIT I TECHNOLOGY-ORIENTED CAD 9

Introduction – Process and Device CAD – Process Simulation Techniques – Interfaces in process and Device CAD – CMOS Technology - Introduction – Ion Implantation – Oxidation – Impurity Diffusion.

UNIT II DEVICE CAD 9

Introduction-Semiconductor Device Analysis – Field-Effect Structures – Bipolar Junction Structures - Introduction – Carrier Densities: Equilibrium case – Non-Equilibrium – Carrier Transport and Conversation – The *pn* Junction – Equilibrium Conditions – The *pn* Junction – Non-equilibrium

UNIT III MOS STRUCTURES 9

Introduction – The MOS capacitor – Basic MOSFET I-V Characteristics – Threshold Voltage in Nonuniform Substrate – MOS Device Design by Simulation.

UNIT IV SENATAURUS TCAD 9

Senataurus TCAD: process simulator – sentaurus process, device simulator –sentaurus device-basic device simulation, advanced concepts – drift-diffusion,hydrodynamic model, stress models.

UNIT V SCRIPTING & SIMULATION 9

Sentaurus TCAD: sentaurus structure editor, meshing concepts, sentaurus work bench, Inspect, Tecplot, Tcl scripting, scheme scripting, Monte-carlo simulation, electro-magnetic simulation.

TOTAL : 45 PERIODS

TEXT BOOKS:

1. Synopsys Sentaurus TCAD Manual, version 2008.09
2. Robert W.Dutton, Zhiping Yu, " Technology CAD Computer Simulation of Processes and Devices", Kluwer Academic Publishers, 1993.
3. M S Lundstorm, Fundamentals of Carrier Transport, 2nd Ed., Cambrid University Press, Cambridge UK, 2000

VL7008 DESIGN OF SEMICONDUCTOR MEMORIES L T P C
3 0 0 3

OBJECTIVES:

1. To study the architectures for SRAM and DRAM
2. To know about various non-volatile memories.
3. To study the fault modelling and testing of memories for fault detection.
4. To lean the radiation hardening process and issues for memory.

UNIT I RANDOM ACCESS MEMORY TECHNOLOGIES 9

Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOI) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs. Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Strucutures-BiCMOS, DRAMs-Soft Error Failures in DRAMs-Advanced DRAM Designs and Architecture-Application, Specific DRAMs.

UNIT II NON VOLATILE MEMORIES 9

Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-BipolarPROMs-CMOS PROMs-Erasable (UV) - Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMs-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Arcitecture-Nonvolatile SRAM-Flash Memories (EPROMs or EEPROM)-Advanced Flash Memory Architecture.

UNIT III MEMORY FAULT MODELING, TESTING, AND MEMORY DESIGN FOR TESTABILITY AND FAULT TOLERANCE 9

RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing Application Specific Memory Testing. General Design for Testability Techniques – Ad Hoc Design Techniques, Structured Design Techniques – RAM Built-In Self – Test (BIST).

UNIT IV RELIABILITY AND RADIATION EFFECTS 9

General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction-Design for Reliability Reliability Test Structures-Reliability creening and Qualification. Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry-Water Level Radiation Testing and Test Structures.

UNIT V PACKAGING TECHNOLOGIES 9

Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability Issues-Memory Cards-High Density Memory Packaging Future Directions.

TOTAL: 45 PERIODS

REFERENCES:
1. Ashok K.Sharma, " Semiconductor Memories Technology, Testing and Reliability ",Prentice-Hall of India Private Limited, New Delhi, 1997.
2. Tegze P.Haraszti, "CMOS Memory Circuits", Kluwer Academic publishers, 2001.
3. Betty Prince, " Emerging Memories: Technologies and Trends", Kluwer Academic publishers, 2002.

AP7071 HARDWARE SOFTWARE CO-DESIGN L T P C
3 0 0 3

OBJECTIVES:
- To study and compare the co-design approaches for single processor and multiprocessor architectures.
- To know the various techniques of prototyping and emulation.
- To study the languages for system level specification and design

UNIT I SYSTEM SPECIFICATION AND MODELLING 9

Embedded Systems, Hardware/Software Co-Design, Co - Design for System Specification and Modelling, Co - Design for Heterogeneous Implementation - Processor Synthesis, Single – Processor Architectures with one ASIC, Single-Processor Architectures with many ASICs, Multi-Processor Architectures, Comparison of Co- Design Approaches, Models of Computation , Requirements for Embedded System Specification .

UNIT II HARDWARE/SOFTWARE PARTITIONING 9

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph , Formulation of the HW/SW Partitioning Problem , Optimization , HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms .

UNIT III HARDWARE/SOFTWARE CO-SYNTHESIS 9

The Co - Synthesis Problem, State - Transition Graph, Refinement and Controller Generation, Distributed System Co-Synthesis

UNIT IV PROTOTYPING AND EMULATION 9

Introduction, Prototyping and Emulation Techniques , Prototyping and Emulation Environments ,Future Developments in Emulation and Prototyping, Target Architecture-Architecture Specialization Techniques ,System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems ,Mixed Systems and Less Specialized Systems

UNIT V DESIGN SPECIFICATION AND VERIFICATION 9

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design System - Level Specification ,Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co- simulation

TOTAL: 45 PERIODS

REFERENCES:
1. Ralf Niemann, "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems", Kluwer Academic Pub, 1998.
2. Jorgen Staunstrup, Wayne Wolf ,"Hardware/Software Co-Design: Principles and Practice" , Kluwer Academic Pub, 1997.
3. Giovanni De Micheli, Rolf Ernst Morgon," Reading in Hardware/Software Co-Design" Kaufmann Publishers, 2001.

CU7001 REAL TIME EMBEDDED SYSTEMS L T P C
3 0 0 3

UNIT I INTRODUCTION TO EMBEDDED COMPUTING 9

Complex systems and microprocessors – Design example: Model train controller – Embedded system design process – Formalism for system design – Instruction sets Preliminaries – ARM Processor – CPU: Programming input and output – Supervisor mode, exception and traps – Coprocessor – Memory system mechanism – CPU performance – CPU power consumption.

UNIT II COMPUTING PLATFORM AND DESIGN ANALYSIS 9

CPU buses – Memory devices – I/O devices – Component interfacing – Design with microprocessors – Development and Debugging – Program design – Model of programs – Assembly and Linking – Basic compilation techniques – Analysis and optimization of execution time, power, energy, program size – Program validation and testing.

UNIT III PROCESS AND OPERATING SYSTEMS 9

Multiple tasks and multi processes – Processes – Context Switching – Operating Systems – Scheduling policies - Multiprocessor – Inter Process Communication mechanisms – Evaluating operating system performance – Power optimization strategies for processes.

UNIT IV HARDWARE ACCELERATES & NETWORKS 9

Accelerators – Accelerated system design – Distributed Embedded Architecture – Networks for Embedded Systems – Network based design – Internet enabled systems.

UNIT V CASE STUDY 9

Hardware and software co-design - Data Compressor - Software Modem – Personal Digital Assistants – Set–Top–Box. – System-on-Silicon – FOSS Tools for embedded system development.

TOTAL: 45 PERIODS

REFERENCES:

1. Wayne Wolf, “Computers as Components - Principles of Embedded Computer System Design”, Morgan Kaufmann Publisher, 2006.
2. David E-Simon, “An Embedded Software Primer”, Pearson Education, 2007.
3. K.V.K.K.Prasad, “Embedded Real-Time Systems: Concepts, Design & Programming”, dreamtech press, 2005.
4. Tim Wilmshurst, “An Introduction to the Design of Small Scale Embedded Systems”, Pal grave Publisher, 2004.
5. Sriram V Iyer, Pankaj Gupta, “Embedded Real Time Systems Programming”, Tata Mc-Graw Hill, 2004.
6. Tammy Noergaard, “Embedded Systems Architecture”, Elsevier, 2006.

VL7009 NANO SCALE TRANSISTORS L T P C
3 0 0 3

OBJECTIVE:

- To understand the necessary of scaling of MOS transistor.
- To introduce the concepts of nanoscale MOS transistor concepts and their performance characteristics.
- To study the various nano scaled MOS transistors.

UNIT I INTRODUCTION TO NOVEL MOSFETS 9

MOSFET scaling, short channel effects-channel engineering - source/drain engineering - high k dielectric - copper interconnects - strain engineering, SOI MOSFET, multigate transistors – single gate – double gate – triple gate – surround gate, quantum effects – volume inversion – mobility – threshold voltage – inter subband scattering, multigate technology – mobility – gate stack

UNIT II PHYSICS OF MULTIGATE MOS SYSTEM 9

MOS Electrostatics – 1D – 2D MOS Electrostatics, MOSFET Current-Voltage Characteristics – CMOS Technology – Ultimate limits, double gate MOS system – gate voltage effect – semiconductor thickness effect – asymmetry effect – oxide thickness effect – electron tunnel current – two dimensional confinement, scattering – mobility

UNIT III NANOWIRE FETS AND TRANSISTORS AT THE MOLECULAR SCALE 9

Silicon nanowire MOSFETs – Evaluvation of I-V characteristics – The I-V characteristics for nondegenerate carrier statistics – The I-V characteristics for degenerate carrier statistics – Carbon nanotubes – Bandstructure of carbon nanotubes – Bandstructure of graphene – Physical structure of nanotubes – Bandstructure of nanotubes – Carbon nanotube FETs – Carbon nanotube MOSFETs – Schottky barrier carbon nanotube FETs – Electronic conduction in molecules – General model for ballistic nanotransistors – MOSFETs with 0D, 1D, and 2D channels – Molecular transistors – Single electron charging – Single electron transistors.

UNIT IV RADIATION EFFECTS 9

Radiation effects in SOI MOSFETs, total ionizing dose effects – single gate SOI – multigate devices, single event effect, scaling effects.

UNIT V CIRCUIT DESIGN USING MULTIGATE DEVICES 9

Digital circuits – impact of device performance on digital circuits – leakage performance trade off – multi VT devices and circuits – SRAM design, analog circuit design – transconductance – intrinsic gain – flicker noise – self heating –band gap voltage reference – operational amplifier – comparator designs, mixed signal – successive approximation DAC, RF circuits.

TOTAL: 45 PERIODS

TEXT BOOKS :

1. J P Colinge, FINFETs and other multi-gate transistors, Springer – Series on integrated circuits and systems, 2008
2. Mark Lundstrom Jing Guo, Nanoscale Transistors: Device Physics, Modeling and Simulation, Springer, 2006.

REFERENCE:

1. M S Lundstorm, Fundamentals of Carrier Transport**,** 2nd Ed., Cambridge University Press, Cambridge UK, 2000

AP7016 SYSTEM ON CHIP DESIGN L T P C
3 0 0 3

OBJECTIVES :

1. To design combinational and sequential logic networks.
2. To learn optimization of power in combinational and sequential logic machines.
3. To study the design principles of FPGA and PLA.
4. To learn various floor planning methods for system design.

UNIT I LOGIC GATES 9

Introduction. Combinational Logic Functions. Static Complementary Gates. Switch Logic. Alternative Gate Circuits. Low-Power Gates. Delay Through Resistive Interconnect. Delay Through Inductive Interconnect. Objectives

UNIT II COMBINATIONAL LOGIC NETWORKS 9

Introduction. Standard Cell-Based Layout. Simulation. Combinational Network Delay. Logic and interconnect Design. Power Optimization. Switch Logic Networks. Combinational Logic Testing.

UNIT III SEQUENTIAL MACHINES 9

Introduction. Latches and Flip-Flops. Sequential Systems and Clocking Disciplines. Sequential System Design. Power Optimization. Design Validation. Sequential Testing.

UNIT IV SUBSYSTEM DESIGN 9

Introduction. Subsystem Design Principles. Combinational Shifters. Adders. ALUs. Multipliers. High-Density Memory. Field Programmable Gate Arrays. Programmable Logic Arrays. References. Problems.

UNIT V FLOOR-PLANNING 9

Introduction, Floor-planning Methods – Block Placement & Channel Definition, Global Routing, switchbox Routing, Power Distribution, Clock Distributions, Floor-planning Tips, Design Validation. Off-Chip Connections – Packages, The I/O Architecture, PAD Design.

TOTAL : 45 PERIODS

REFERENCES

1. Wayne Wolf, “Modern VLSI Design – System – on – Chip Design”, Prentice Hall, 3rd Edition, 2008.
2. Wayne Wolf , “Modern VLSI Design – IP based Design”, Prentice Hall, 4th Edition, 2008.

CP7023 RECONFIGURABLE COMPUTING L T P C
3 0 0 3

OBJECTIVES:

- To understand the need for reconfigurable computing
- To expose the students to various device architectures
- To examine the various reconfigurable computing systems
- To understand the different types of compute models for programming reconfigurable architectures
- To expose the students to HDL programming and familiarize with the development environment
- To expose the students to the various placement and routing protocols
- To develop applications with FPGAs

UNIT I DEVICE ARCHITECTURE 9

General Purpose Computing Vs Reconfigurable Computing – Simple Programmable Logic Devices – Complex Programmable Logic Devices – FPGAs – Device Architecture - Case Studies.

UNIT II RECONFIGURABLE COMPUTING ARCHITECTURES AND SYSTEMS 9

Reconfigurable Processing Fabric Architectures – RPF Integration into Traditional Computing Systems – Reconfigurable Computing Systems – Case Studies – Reconfiguration Management.

UNIT III PROGRAMMING RECONFIGURABLE SYSTEMS 9

Compute Models - Programming FPGA Applications in HDL – Compiling C for Spatial Computing – Operating System Support for Reconfigurable Computing.

UNIT IV MAPPING DESIGNS TO RECONFIGURABLE PLATFORMS 9

The Design Flow - Technology Mapping – FPGA Placement and Routing – Configuration Bitstream Generation – Case Studies with Appropriate Tools.

UNIT V APPLICATION DEVELOPMENT WITH FPGAS 9

Case Studies of FPGA Applications – System on a Programmable Chip (SoPC) Designs.

TOTAL: 45 PERIODS

OUTCOMES:

Upon completion of the course, the students will be able to

- Identify the need for reconfigurable architectures
- Discuss the architecture of FPGAs
- Point out the salient features of different reconfigurable architectures
- Build basic modules using any HDL
- Develop applications using any HDL and appropriate tools
- Design and build an SoPC for a particular application

REFERENCES:

1. Maya B. Gokhale and Paul S. Graham, "Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays", Springer, 2005.
2. Scott Hauck and Andre Dehon (Eds.), "Reconfigurable Computing – The Theory and Practice of FPGA-Based Computation", Elsevier / Morgan Kaufmann, 2008.
3. Christophe Bobda, "Introduction to Reconfigurable Computing – Architectures, Algorithms and Applications", Springer, 2010.

VL7010 SUBMICRON VLSI DESIGN L T P C
3 0 0 3

OBJECTIVES:

- To introduce the concepts of Silicon realization of ASIC and cmos devices at deep submicron level.
- To study and apply the deep submicron concepts to cmos low power devices.
- To study and discuss about RF CMOS transistor sizing and its limitations.

UNIT I SILICON REALIZATION OF ASIC 9

Introduction-Handcrafted layout implementation-bit-slice layout implementation-Cell based layout implementation- gate array layout implementation-Hierchial design approach- The choice of layout implementation form

UNIT II LOW POWER DESIGN 9

Sources of CMOS power consumption-technology options for low power-reduction of P-leak by technological measures Reduction of P-dyn by technology measures-reduction of P-dyn by reduced voltage process-design option for low power-computing power vs chip power-a scaling perspectives.

UNIT III DESIGN FOR RELIABILITY 9

Introduction-latch up in CMOS circuits-Electrostatics discharge-and its protection-Electro migration-Hot carrier degradation design for signal integrity-clock distribution and critical timing issues-clock generation and synchronization in different domain on a chip-the influence of interconnection-design organization

UNIT IV DEEP SUB MICRON 9

RF CMOS Transistor downsizing limitations-. RF basic blocks layout implementation Submicron technology and layout dependent effects-input output interfacing, the bonding pad, the pad ring, electrostatic discharge prevention,

UNIT V CMOS DEVICES 9

Clamp CMOS devices, zener diode-input structure-output structure-pull up-pull down-i/o pad, power clamp-core/pad limitation I/O Pad description using Ibis-Connecting to the package-Signal propagation between integrated circuits

TOTAL: 45 PERIODS

REFERENCES:

1. Deep-Submicron Cmos Ics: From Basics to Asics By Harry J. M. Veendrick
2. Low Power Design in Deep Submicron Electronics by W. Nebel, Jean P. Mermet
3. Low-Power Deep Sub-Micron CMOS Logic: Sub-threshold Current Reduction by P.R. Van Der Meer, Arie van Staveren, Arthur H. M. van Roermund

AP7301 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY L T P C
3 0 0 3

OBJECTIVES:

- To understand the basics of EMI
- To study EMI Sources
- To understand EMI problems
- To understand Solution methods in PCB
- To understand Measurement technique for emission
- To understand Measurement technique for immunity

UNIT I EMI/EMC CONCEPTS 9

EMI-EMC definitions and Units of parameters; Sources and victim of EMI; Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

UNIT II EMI COUPLING PRINCIPLES 9

Conducted, radiated and transient coupling; Common ground impedance coupling ; Common mode and ground loop coupling ; Differential mode coupling; Near field cable to cable coupling, cross talk ; Field to cable coupling ; Power mains and Power supply coupling.

UNIT III EMI CONTROL TECHNIQUES 9

Shielding- Shielding Material-Shielding integrity at discontinuties, Filtering- Characteristics of Filters-Impedance and Lumped element filters-Telephone line filter, Power line filter design, Filter installation and Evaluation, Grounding- Measurement of Ground resistance-system grounding for EMI/EMC-Cable shielded grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control. EMI gaskets

UNIT IV EMC DESIGN OF PCBS 9

EMI Suppression Cables-Absorptive, ribbon cables-Devices-Transient protection hybrid circuits ,Component selection and mounting; PCB trace impedance; Routing; Cross talk control-Electromagnetic Pulse-Noise from relays and switches, Power distribution decoupling; Zoning; Grounding; VIAs connection; Terminations.

UNIT V EMI MEASUREMENTS AND STANDARDS 9

Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer; Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462. Frequency assignment - spectrum conversation. British VDE standards, Euro norms standards in japan - comparisons. EN Emission and Susceptibility standards and Specifications.

TOTAL: 45PERIODS

OUTCOMES

Upon Completion of the course, the students will be able to

- To design a EMI free system
- To reduce system level crosstalk
- To design high speed Printed Circuit board with minimum interference
- To make our world free from unwanted electromagnetic environment

REFERENCES:

1. V.P.Kodali, “Engineering EMC Principles, Measurements and Technologies”, IEEE Press, New York, 1996.
2. Clayton R.Paul,” Introduction to Electromagnetic Compatibility”, John Wiley Publications, 2008
3. Henry W.Ott., ”Noise Reduction Techniques in Electronic Systems”, A Wiley Inter Science
4. Publications, John Wiley and Sons, Newyork, 1988.
5. Bemhard Keiser, “Principles of Electromagnetic Compatibility”, 3rd Ed, Artech house, Don R.J. White Consultant Incorporate, “Handbook of EMI/EMC” , Vol I-V, 1988.

VL7011 SIGNAL INTEGRITY FOR HIGH SPEED DEVICES

L	T	P	C
3	0	0	3

OBJECTIVES:

1. To learn the fundamental and importance of signal integrity.
2. To analyze and minimize cross talk in unbounded conductive media.
3. To study about the different types of Di-Electric materials.
4. To learn about differential cross talk and CMOS based transmission line model

UNIT I FUNDAMENTALS **9**

The importance of signal integrity-new realm of bus design-Electromagnetic fundamentals for signal integrity-maxwell equations common vector operators-wave propagations-Electrostatics-magneto statics-Power flow and the poynting vector-Reflections of electromagnetic waves

UNIT II CROSS TALK **9**

Introduction -mutual inductance and capacitance-coupled wave equation-coupled line analysis-modal analysis-cross talk minimization signal propagation in unbounded conductive media-classic conductor model for transmission model

UNIT III DI-ELECTRIC MATERIALS **9**

Polarization of Dielectric-Classification of Di electric material-frequency dependent di electric material- Classification of Di electric material fiber-Weave effect-Environmental variation in di electric behaviour Transmission line parameters for loosy dielectric and realistics conductors

UNIT IV DIFFERENTIAL SIGNALING **9**

Removal of common mode noise-Differential Cross talk-Virtual reference plane-propagation of model voltages common terminology-drawbacks of Differential signaling

UNIT V PHYSICAL TRANSMISSION LINE MODEL **9**

Introduction- non ideal return paths-Vias-IO design consideration-Push-pull transmitter-CMOS receivers-ESSD protection circuits-On chip Termination

TOTAL:45 PERIODS

REFERENCES:

1. Advanced Signal Integrity for High-Speed Digital Designs By Stephen H. Hall, Howard L. Heck
2. Signal and power integrity in digital systems: TTL, CMOS, and BiCMOS by James Edgar Buchanan

VL7012 MIXED SIGNAL IC TEST AND MEASUREMENTS L T P C
3 0 0 3

OBJECTIVES:

- To know about mixed-signal devices and the need for testing these devices.
- To study the various techniques for testing.
- To learn about DSP based testing.
- To understand the benefits and techniques of DFT.
- To study the general purpose measuring devices.

UNIT I OVERVIEW OF MIXED – SIGNAL TESTING 9

MIXED – SIGNAL CIRCUITS Common Types of Analog and Mixed- Signal Circuits – Applications of Mixed-Signal Circuits - The CMOS Fabrication process – Real –World Circuits – What Is a Test Engineer Post Silicon Production Flow-Test and Packing – Characterization versus Production Testing Test and Diagnostic Equipments-Automated Test Equipments – Wafer Probers – Handlers – E-Beam Probers – Focused Ion Beam Equipments – Forced -Temperature

UNIT II DC AND PARAMETRIC MEASUREMENT 9

Purpose of Continuity Testing – Continuity Test Techniques – Serial Versus Parallel Continuity Testing Purpose of Leakage Testing – Leakage Test Technique – Serial versus Parallel Leakage Testing Importance of Supply current tests – Test Techniques Voltage Regulators – Voltage References – Trimmable References Input Impedance – Output Impedance – Differential Impedance Measurements V_{MID} and Analog Ground - DC transfer Characteristics (Gain and Offset) – Output Offset Voltage (Vo) – Single-Ended, Differential and Common-Model Offsets – Input Offset Voltage (Vos) Closed-Loop Gain – Open – Loop Gain DC power supply sensitivity – DC Power Supply Rejection Ration

UNIT III TESTER HARDWARE 9

General-Purpose Tester versus Focused Bench Equipment – Generic Tester Architecture General-Purpose Multimeters – General-Purpose Voltage/Current Sources – Precision Voltage References and User Supplies – Calibration Source – Relay Matrices – Relay Control Lines Digital Vectors – Digital Signals – Source Memory – Capture Memory - Pin Card Electronics – Timing and Formatting Electronics AC Continuous Wave source and AC Meter – Arbitrary Waveform Generators- Waveform Digitizers – Clocking and Synchronization Time Measurements – Time Measurement Interconnects

UNIT IV DSP – BASED TESTING 9

Reduced Test Time – Separation of Signal Components – Advanced Signal Manipulations DSP and Array Processing – Fourier Analysis of Periodic Signals – The Trigonometric Fourier Series – The Discrete- Time Fourier Series – Complete Frequency Renormalization The Discrete Fourier Transform – The Fast Fourier Transform – Interpreting the FFT Output Equivalence of Time- and Frequency – Domain Information – Parseval's Theorem – Applications of the Inverse FFT – Frequency – Domain Filtering – Noise Weighting

UNIT V DESIGN FOR TEST (DFT) 9

Built- In Self-Test – Differences between Digital Dft and Analog Dft Lower Cost of Test – Increased Fault Coverage and Improved Process Control – Diagnostics and Characterization – Diagnostics and Characterization – Ease of Test Program Development- System- Level Diagnostics – Economics of DfT Scan Basics – IEEE Std. 1149. 1 Standard Test Access Port and Boundary Scan – Full Scan and Partial Scan Pseudorandom BILBO Circuits – Memory BIST – Microcode BIST Partitioning – Digital Resets and Presets – Device-Driven Timing – Lengthy Preambles Mixed – Signal Boundary Scan (IEEE Std. 1149.4) - Analog and Mixed-Signal BIST

TOTAL:45 PERIODS

REFERENCES:

1. An Introduction to Mixed-signal IC Test and Measurement by Gordon W.Roberts, Friedrich Taenzler, Mark Burns
2. Analog and mixed-signal test by Bapiraju Vinnakota
3. Digital and Analogue Instrumentation: Testing and Measurement by Nihal Kularatna

AP7010 DATA CONVERTERS L T P C
3 0 0 3

OBJECTIVE:

- To study the A/D and D/A architectures
  To study the importance of sample and hold circuits in A/D and D/A conversion techniques.

UNIT I SAMPLE AND HOLD CIRCUITS 9

Sampling switches, Conventional open loop and closed loop sample and hold architecture, Open loop architecture with miller compensation, multiplexed input architectures, recycling architecture switched capacitor architecture.

UNIT II SWITCHED CAPACITOR CIRCUITS AND COMPARATORS 9

Switched-capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators.

UNIT III DIGITAL TO ANALOG CONVERSION 9

Performance metrics, reference multiplication and division, switching and logic functions in DAC, Resistor ladder DAC architecture, current steering DAC architecture.

UNIT IV ANALOG TO DIGITAL CONVERSION 9

Performance metric, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture.

UNIT V PRECISION TECHNIQUES 9

Comparator offset cancellation, Op Amp offset cancellation, Calibration techniques, range overlap and digital correction.

TOTAL:45 PERIODS

REFERENCE:

1. Behzad Razavi, “Principles of data conversion system design”, S. Chand and company Ltd, 2000.

VL7013 VLSI FOR WIRELESS COMMUNICATION L T P C
3 0 0 3

OBJECTIVES:

- To study the design concepts of low noise amplifiers.
- To study the various types of mixers designed for wireless communication.
- To study and design PLL and VCO.
- To understand the concepts of CDMA in wireless communication.

UNIT I COMPONENTS AND DEVICES 9

Integrated inductors, resistors, MOSFET and BJT AMPLIFIER DESIGN: Low Noise Amplifier Design - Wideband LNA - Design Narrowband LNA - Impedance Matching - Automatic Gain Control Amplifiers – Power Amplifiers

UNIT II MIXERS 9

Balancing Mixer - Qualitative Description of the Gilbert Mixer - Conversion Gain – Distortion - Low Frequency Case: Analysis of Gilbert Mixer – Distortion - High-Frequency Case – Noise - A Complete Active Mixer. Switching Mixer - Distortion in Unbalanced Switching Mixer - Conversion Gain in Unbalanced Switching Mixer - Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain in Single Ended Sampling Mixer - Distortion in Single Ended Sampling Mixer - Intrinsic Noise in Single Ended Sampling Mixer - Extrinsic Noise in Single Ended Sampling Mixer.

UNIT III FREQUENCY SYNTHESIZERS 9

Phase Locked Loops - Voltage Controlled Oscillators - Phase Detector – Analog Phase Detectors – Digital Phase Detectors - Frequency Dividers - LC Oscillators - Ring Oscillators - Phase Noise - A Complete Synthesizer Design Example (DECT Application).

UNIT IV UB SYSTEMS 9

Data converters in communications, adaptive Filters, equalizers and transceivers

UNIT V IMPLEMENTATIONS 9

VLSI architecture for Multitier Wireless System - Hardware Design Issues for a Next generation CDMA System .

TOTAL:45 PERIODS

REFERENCES:

1. B.Razavi ,"RF Microelectronics" , Prentice-Hall ,1998.
2. Bosco H Leung "VLSI for Wireless Communication", Pearson Education, 2002.
3. Thomas H.Lee, "The Design of CMOS Radio –Frequency Integrated Circuits', Cambridge University Press ,2003.
4. Emad N Farag and Mohamed I Elmasry, "Mixed Signal VLSI Wireless Design - Circuits and Systems", Kluwer Academic Publishers, 2000.
5. Behzad Razavi, "Design of Analog CMOS Integrated Circuits" McGraw-Hill, 1999.
6. J. Crols and M. Steyaert, "CMOS Wireless Transceiver Design," Boston, Kluwer Academic Pub., 1997.

VL7014 IP BASED VLSI DESIGN L T P C
3 0 0 3

OBJECTIVES:

- To learn about IC manufacturing and fabrication
- To analyse the combinational, sequential and subsystem design
- To study about different floor planning techniques and architecture design
- To have an introduction to IP design security

UNIT I VLSI AND ITS FABRICATION 9

Introduction, IC manufacturing, CMOS technology, IC design techniques, IP based design, Fabrication process-Transistors, Wires and Via, Fabrication Theory reliability, Layout Design and tools.

UNIT II COMBINATIONAL LOGIC NETWORKS 9

Logic Gates: Combinational Logic Functions, Static Complementary Gates, Switch Logic, Alternate Gate circuits, Low power gates, Delay, Yield, Gates as IP, Combinational Logic Networks-Standard Cell based Layout, Combinational network delay, Logic and Interconnect design, Power optimization, Switch logic network, logic testing;

UNIT III SUBSYSTEM DESIGN 9

Sequential Machine-Latch and Flip flop, System design and Clocking, Performance analysis, power optimization, Design validation and testing; Subsystem Design-Combinational Shifter, Arithmetic Circuits, High Density memory, Image Sensors, FPGA,PLA, Buses and NoC, Data paths, Subsystems as IP.

UNIT IV FLOOR PLANNING AND ARCHITECTURE DESIGN 9

Floor planning-Floor planning methods, Global Interconnect, Floor plan design, Off-chip Connections Architecture Design- HDL, Register-Transfer Design, Pipelining, High Level Synthesis, Architecture for Low power, GALS systems, Architecture Testing, IP Components, Design Methodologies, Multiprocessor System-on-chip Design

UNIT V DESIGN SECURITY **9**

IP in reuse based design, Constrained based IP protection, Protection of data and Privacy-constrained based watermarking for VLSI IP based protection

TOTAL:45 PERIODS

REFERENCES:

1. Wayne wolf, “Modern VLSI Design:IP-based Design”, Pearson Education,2009.
2. Qu gang, Miodrag potkonjak, “Intellectual Property Protection in VLSI Designs: Theory and Practice”, kluwer academic publishers,2003.

VL7015 NANOSCALE DEVICES AND CIRCUIT DESIGN **L T P C**
3 0 0 3

OBJECTIVES:

1. To learn about leakage current and its control and reduction techniques in CMOS devices.
2. To know the device technologies for sub 100nm CMOS.
3. To study the device scaling of single and multigate MOSFETs.
4. To familiarize the low power design and voltage scaling issues in Nano scale devices.
5. To study about various nanoscale devices.
6. To design CMOS circuit using non-classical devices**.**

UNIT I CMOS SCALING CHALLENGES IN NANOSCALE REGIMES **9**

Leakage current mechanisms in nanoscale CMOS, leakage control and reduction techniques, process variations in devices and interconnects. **Device technologies for sub 100nm CMOS:** Silicidation and Cu-low k interconnects, strain silicon – biaxial stain and process induced strain; Metal-high k gate; Emerging CMOS technologies at 32nm scale and beyond – FINFETs, surround gate nanowire MOSFETs, heterostructure (III-V) and Si-Ge MOSFETs.

UNIT II DEVICE SCALING AND BALLISTIC MOSFET **9**

Two dimensional scaling theory of single and multigate MOSFETs, generalized scale length, quantum confinement and tunneling in MOSFTEs, velocity saturation, carrier back scattering and injection velocity effects, scattering theory of MOSFETs.

UNIT III EMERGING NANOSCALE DEVICES **9**

Si and hetero-structure nanowire MOSFETs, carbon nanotube MOSFETs, quantum wells, quantum wires and quantum dots; Single electron transistors, resonant tunneling devices.

UNIT IV NANOSCALE CMOS DESIGN **9**

CMOS logic power and performance, voltage scaling issues; Introduction to low power design; Performance optimization for data paths.

UNIT V NANOSCALE CIRCUITS **9**

Statistical circuit design, variability reduction, design for manufacturing and design optimization; Sequential logic circuits, registers, timing and clock distribution, IO circuits and memory design and trends. **Non-classical CMOS**: CMOS circuit design using non-classical devices – FINFETs, nanowire, carbon nanotubes and tunnel devices.

TOTAL : 45 PERIODS

REFERENCES:

1. Lundstrom, M., “Nanoscale Transport: Device Physics, Modeling, and Simulation”, Springer. 2000
2. Maiti, C.K., Chattopadhyay, S. and Bera, L.K., “Strained-Si and Hetrostructure Field Effect Devices”, Taylor and Francis, 2007
3. Hanson, G.W., “Fundamentals of Nanoelectronics”, Pearson, India., 2008.
4. Wong, B.P., Mittal, A., Cao Y. and Starr, G., “Nano-CMOS Circuit and Physical Design”, Wiley, 2004
5. Lavagno, L., Scheffer, L. and Martin, G., “EDA for IC Implementation Circuit Design and Process Technology”, Taylor and Francis, 2005