

KCG

COLLEGE OF TECHNOLOGY

AFFILIATED TO ANNA UNIVERSITY | AUTONOMOUS

REGULATION - 2023

CURRICULUMAND SYLLABI

M.E VLSI Design

KCGCollegeofTechnologywasfoundedin1998tofulfillthe Founder-Chairman,Dr.KCGVerghese'svisionof**"ToMake EveryManaSuccessandNoManaFailure".**It isa Christian minority institution, affiliated to Anna University (Autonomous),Chennai and approved byAICTE, NewDelhi.

VISIONOFKCG

KCG College of Technology aspires to become a globally recognized centre of excellence for science, technology & engineering education, committed to quality teaching, learning and research while ensuring for every student a unique educational experience which will promote leadership, job creation, social commitment and service to nation building.

MISSIONOFKCG

- Disseminate knowledge in a rigorous and intellectually stimulating environment.
- Facilitatesociallyresponsiveresearch,innovationandentrepreneurship.
- Foster holistic development and professional competency.
- Nurturethevirtueofserviceandanethicalvaluesystem in the young minds.

VISION OF ELECTRONICS AND COMMUNICATION ENGINEERING

To become a center of excellence of global significance in Electronics and Communication engineering and producing competent professionals committed to nation building.

MISSION OF ELECTRONICS AND COMMUNICATION ENGINEERING

Provide quality education in the field of Electronics and Communication Engineering & related domains

- Impart strong knowledge in the field of Electronics and Communication engineering through innovative teaching and learning process
- Establish laboratories equipped with modern state of art technology resources to facilitate research andconsultancy
- Enhance the knowledge and skills of the faculty to incorporate the latest advancements
- Facilitate Industrial collaboration in socially responsive research activities

PROGRAMMEEDUCATIONAL OBJECTIVES (PEOS)

Thegraduateswill:

PEO1	Have a successful career as technically competent, highly skilled professionals in Electronics and communication engineering and its related fields
PEO2	Demonstrate technical competence to provide solutions for real time Electronics and Communication engineering problems
PEO3	Adopt technological challenges through skill upgradation in the relevant areas
PEO4	Exhibit professionalism and ethical attitude in theirwork

PROGRAMOUTCOMES(POs)

Engineeringgraduateswillbeableto:

PO01	An ability to independently carry out research/investigation and development workto solve practical problems.
PO02	An ability to write and present a substantial technical report/document.
PO03	Students should be able to demonstrate a degree of mastery over the area as per thespecialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.
PO04	An ability to analyze, design, simulate, verify, and optimize complex VLSI systems using modern Electronic Design Automation (EDA) tools and advancedsemiconductor technologies.
PO05	An ability to apply advanced engineering knowledge and research methodologies todevelop innovative, sustainable, and industry-relevant VLSI solutions foraddressing real-world engineering challenges.
PO06	An ability to function effectively as an individual or as a member ofmultidisciplinary teams while demonstrating professional ethics, effectivecommunication, leadership, and lifelong learning in the field of VLSI Design.

PROGRAMSPECIFICOUTCOMES(PSOs)

PSO01	An ability to analyze, design, verify, and optimize complex VLSI circuits using modern Electronic Design Automation (EDA) tools and semiconductor technologies.
PSO02	An ability to develop and evaluate System-on-Chip (SoC) architectures and embedded hardware solutions using advanced design and verification methodologies.
PSO03	An ability to investigate emerging VLSI technologies and develop innovative, research-oriented solutions for industrial and societal applications.

AUTONOMOUSCOLLEGESAFFILIATED ANNAUNIVERSITY
M.E. VLSI DESIGN
REGULATIONS–2023
CHOICEBASEDCREDITSYSTEM
ITOIVSEMESTERSCURRICULAAND1st SEMESTERSYLLABI

SEMESTERI

SL. NO	COURSE CODE	COURSETITLE	CATE GORY	PERIODS PERWEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	23VDP101	SemiconductorDeviceModellingand Simulation	FC	2	0	2	4	3
2.	23RMP101	ResearchMethodologyandIPR	MC	2	1	0	3	3
3.	23VDP102	DigitalCMOSVLSIDesign	PCC	3	0	0	3	3
4.	23VDP103	AnalogIntegratedCircuit Design	PCC	3	0	4	7	5
5.	23VDP104	VLSIDigitalSignalProcessing	PCC	3	0	0	3	3
6.	23VDP105	HardwareDescriptionLanguagesfor RTLDesigns	PCC	3	0	4	7	5
TOTAL				**16**	**1**	**10**	**27**	**22**

SEMESTERII

SL. NO	COURSE CODE	COURSETITLE	CATE GORY	PERIODS PERWEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1.	23VDP201	DesignforVerificationusingUVM	PCC	3	0	0	3	3
2.	23VDP202	LowPowerVLSIDesign	PCC	3	0	4	7	5
3.	23VDP203	CADforVLSIDesign	PCC	3	0	0	3	3
4.	23VDP0xx	ProfessionalElectiveI	PEC	3	0	0	3	3
5.	23VDP0xx	ProfessionalElectiveII	PEC	3	0	0	3	3
PRACTICAL								
6.	23VDP221	VerificationusingUVMLaboratory	PCC	0	0	4	4	2
7.	23VDP222	TermPaperWritingandSeminar	EEC	0	0	4	4	2
TOTAL				**15**	**0**	**12**	**27**	**21**

SEMESTERIII

SL. NO	COURSE CODE	COURSETITLE	CATE GORY	PERIODS PERWEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
THEORY								
1	23VDP0xx	ProfessionalElectiveIII	PEC	3	0	0	3	3
2	23VDP0xx	ProfessionalElectiveIV	PEC	3	0	0	3	3
3	23VDP0xx	ProfessionalElectiveV	PEC	3	0	2	5	4
PRACTICAL								
4	23VDP321	ProjectWorkI	EEC	0	0	12	12	6
TOTAL				**9**	**0**	**14**	**23**	**16**

SEMESTER IV

SL. NO	COURSE CODE	COURSETITLE	CATE GORY	PERIODS PERWEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
PRACTICAL								
1	23VDP421	ProjectWorkII	EEC	0	0	24	24	12
TOTAL				**0**	**0**	**24**	**24**	**12**

TOTALNO.OFCREDITS:71

FOUNDATIONCOURSES(FC)

SL. NO	COURSE CODE	COURSETITLE	CATE GORY	PERIODS PERWEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	23VDP101	SemiconductorDeviceModeling andSimulation	FC	2	0	2	4	3

PROFESSIONALCORECOURSES(PCC)

SI. NO	COURSE CODE	COURSETITLE	CATEGORY	PERIODS PERWEEK			CONTACT PERIODS	CREDITS
				L	T	P		
1.	23VDP102	DigitalCMOSVLSI Design	PCC	3	0	0	3	3
2.	23VDP103	AnalogIntegratedCircuitDesign	PCC	3	0	4	7	5
3.	23VDP104	VLSIDigitalSignalProcessing	PCC	3	0	0	3	3
4.	23VDP105	HardwareDescriptionLanguages for RTLDesigns	PCC	3	0	4	7	5
5.	23VDP201	DesignforVerificationusingUVM	PCC	3	0	0	3	3
6.	23VDP202	LowPowerVLSI Design	PCC	3	0	4	7	5
7.	23VDP203	CADforVLSIDesign	PCC	3	0	0	3	3
8.	23VDP221	VerificationusingUVMLaboratory	PCC	0	0	4	4	2

PROFESSIONALELECTIVECOURSE(PEC)

S. NO.	COURSE CODE	COURSETITLE	CATE-GORY	PERIODS PERWEEK			TOTAL CONTACT PERIODS	CREDITS
				L	T	P		
1.	23VDP041	ASICDesign	PEC	3	0	0	3	3
2.	23VDP042	EmbeddedSystemDesign	PEC	3	0	0	3	3
3.	23VDP043	ElectromagneticInterference andCompatibility	PEC	3	0	0	3	3
4.	23VDP044	DataConverters	PEC	3	0	0	3	3
5.	23VDP045	HardwareSoftwareCo-DesignforFPGA	PEC	3	0	0	3	3
6.	23VDP046	PowerManagementandClock Distribution Circuits	PEC	3	0	0	3	3
7.	23VDP047	ReconfigurableArchitectures	PEC	3	0	0	3	3
8.	23VDP048	AdvancedWirelessSensor Networks	PEC	3	0	0	3	3
9.	23VDP049	SignalIntegrityforHighSpeed Design	PEC	3	0	0	3	3
10.	23VDP050	SystemOnChip	PEC	3	0	0	3	3
11.	23VDP051	MEMSandNEMS	PEC	3	0	0	3	3
12.	23VDP052	NetworkonChip	PEC	3	0	0	3	3
13.	23VDP053	Nanotechnology	PEC	3	0	0	3	3
14.	23VDP054	EvolvableHardware	PEC	3	0	0	3	3
15.	23VDP055	QuantumComputing	PEC	3	0	0	3	3
ProfessionalElectiveIV - VLSI Systems and Hardware Design								
16.	23VDP056	Soft Computing and Optimization Techniques	PEC	3	0	2	5	4
17.	23VDP057	VLSI for Wireless Communication	PEC	3	0	2	5	4
18.	23VDP058	Pattern Recognition	PEC	3	0	2	5	4
19.	23VDP059	System Verilog	PEC	3	0	2	5	4
20.	23VDP060	Machine Learning	PEC	3	0	2	5	4
Professional Elective V - Intelligent Signal Processing and AI								
21.	23VDP061	AdaptiveSignalProcessing	PEC	3	0	2	5	4
22.	23VDP062	VLSI Architectures for Image Processing	PEC	3	0	2	5	4
23.	23VDP063	DSP Structures for VLSI	PEC	3	0	2	5	4
24.	23VDP064	Bio Signal Processing	PEC	3	0	2	5	4
25.	23VDP065	DigitalImageandVideo Processing	PEC	3	0	2	5	4

RESEARCHMETHODOLOGYANDIPRCOURSES(RMC)

S. NO	COURSE CODE	COURSETITLE	PERIODS PERWEEK			CREDITS	SEMESTER
			L	T	P		
1.	23RMP101	ResearchMethodologyandIPR	2	1	0	3	1
TOTAL CREDITS						3	

EMPLOYABILITYENHANCEMENTCOURSES(EEC)

SI.NO	COURSE CODE	COURSETITLE	CATEGORY	PERIODS PERWEEK			CONTACT PERIODS	CREDITS
				L	T	P		
1.	23VDP222	TermPaperWritingand Seminar	EEC	0	0	4	4	2
2.	23VDP321	ProjectWorkI	EEC	0	0	12	12	6
3.	23VDP421	ProjectWorkII	EEC	0	0	24	24	12

SummaryCreditDistributionforVariousCategoryofCoursebySemesterWise

M.E.VLSIDESIGN						
S.No	SubjectArea	Creditsper Semester				Credits Total
		I	II	III	IV	
1	FC	3				3
2	PCC	16	13			29
3	PEC		6	10		16
4	MC	3				3
5	EEC		2	6	12	20
	Total	22	21	16	12	71

23VDP101 SEMICONDUCTORDEVICEMODELINGANDSIMULATION LTPC 2023

UNIT I BASICTHEORYOFSEMICONDUCTORS 6

Introduction, - direct and indirect semiconductors – Fermi-Dirac statistics - Quasi-Fermi Levels - Poisson's Equation, conduction in semiconductor, effect of temperature, doping, and high electric field on carrier mobility, PN junction at equilibrium - current-voltage characteristics-diode current model and its limitations

UNITII MOSFETDEVICEPHYSICS 6

MOS capacitor – potential balance and charge balance, the effect of gate-body voltage – MOSFET structures - qualitative description of MOS transistor operation – MOS transistor characteristics – Transistor regions of operations – CMOS fabrication process.

UNITIII MOSFETSTATICMODELS 6

Static drain current model – simple charge controlmodel - Pao-Sah model - Pierret-Shields's model – charge sheet model – strong inversion model – weak inversion model – SPICE model, short channeleffects,Quantummechanicaleffects,modelingoflightlydopeddrainMOSFETandSOI MOSFET.

UNITIV MODELINGFORCIRCUITSIMULATORS 6

Introduction, types of models, attributes for good compact models, model formulation, model implementation in circuitsimulators, modeltesting, parameter extraction, simulation, and extraction forRFapplications,compactmodels– BSIMmodels- EKVmodels– PSPmodels.

UNITV DEVICESCALING ANDVARIABILITYEFFECTS 6

Introduction, classical scaling laws, process variability- global and local process variability, characterization of parametric variability in MOSFETs, Reliability of MOSFETs - high-field effects, hot carrier degradation, bias temperature instability, MOSFET breakdown, high-k dielectrics.

TOTAL:30PERIODS

LABEXPERIMENTS:

SimulationsusingMATLAB/TCAD/EquivalentOpen-Sourcetools

1. Simulationoftransfercharacteristics(I_{DS}vsV_{GS})ofMOSFET
2. Simulationofdraincharacteristics(I_{DS}vsV_{DS})ofMOSFET
3. Extractionofthresholdvoltage,transconductance,deviceONandOFFcurrent,and subthreshold slope of MOSFET
4. Numericalsimulationofdraincurrentcharacteristics ofMOSFET

Simulationsusing SPICEtools

5. SimulationoftransferanddraincharacteristicsofNMOSandPMOStransistorsusing Verilog-A based BSIM4 models
6. SimulationofvoltagetransfercharacteristicsofCMOSinverterusingVerilog-AbasedBSIM SOI models
7. Simulationofshortchanneleffectssuchasthresholdvoltageroll-offandDIBLeffectsof nano-scaled MOSFET using the model card
8. SimulationofvariationsofMOSFET transfercharacteristicsduetoprocessvariabilityeffects

9. SimulationofNMOStransistorsincorporatingthehot-carriereffectsusingsub-circuit modules
10. SimulationofPMOStransistorsincorporatingthenegativebiastemperatureinstabilityusing sub-circuit modules

TOTAL:60PERIODS

COURSEOUTCOMES:

Attheendofthecourse,thestudentwillbeableto:

CO1:Apply the semiconductorconcepts ofdrift,diffusion,donors andacceptors, majority and minority carriers, and carrier mobility
CO2:Illustratethephysicsandprinciplesofoperationofp-njunctiondiodes,MOScapacitors,and MOSFETs
CO3:DesignandsimulateMOSFETdevices,takingintoconsiderationofnon-idealandshort-channel effects
CO4:Developcompact modelsforshort-channelMOSFETssuitableforSPICEsimulators
CO5:Analyzetheprocessvariabilityandreliabilityeffectsofthenano-scaledMOSFETsand simulate the device lifetime.

REFERENCES:

1. Tsividis,Y.&McAndrew,C.Operation,andmodelingoftheMOStransistor.Thirdedition, Oxford University Press, USA: 2015.
2. ABBhattacharyya,"CompactMOSFETmodelsforVLSIdesign",Wiley,NewYork,2016.
3. J.J.Liou,A.Ortiz-Conde,F.Garcia-Sanchez,"AnalysisandDesignofMOSFETs:Modeling, Simulation, and Parameter Extraction", Springer Science & Business Media, 2015.
4. K.Saha,"Compactmodelsforintegratedcircuitdesign:Conventionaltransistorsand beyond", Taylor & Francis, 2015**.**
5. T.Ytterdal,Y.Cheng,T.A.Fjeldly,"DeviceModelingforAnalogandRFCMOSCircuit Design", John Wiley & Sons, New York 2015.

23RTMP101 RESEARCHMETHODOLOGYANDIPR L TP C
2 1 0 3

UNITI RESEARCHPROBLEMFORMULATION **9**

Objectives of research, types of research, research process, approaches to research; conducting literaturereview-informationsources,informationretrieval,toolsforidentifyingliterature, Indexing andabstractingservices,Citationindexes,summarizingthereview,criticalreview,identifying research gap, conceptualizing and hypothesizing the research gap

UNITII RESEARCHDESIGNANDDATACOLLECTION **9**

Statisticaldesignofexperiments-typesandprinciples;datatypes&classification;datacollection - methods and tools

UNITIII DATAANALYSIS,INTERPRETATIONANDREPORTING **9**

Sampling,samplingerror,measuresofcentraltendencyandvariation,;testofhypothesis-concepts; data presentation- types of tables and illustrations; guidelines for writing the abstract, introduction, methodology, results and discussion, conclusion sections of a manuscript; guidelines for writing thesis, research proposal; References – Styles and methods, Citation and listing system of documents; plagiarism, ethical considerations in research

UNITIV INTELLECTUALPROPERTYRIGHTS **9**

Concept of IPR, types of IPR – Patent, Designs, Trademarks and Trade secrets, Geographical indications, Copy rights, applicability of these IPR; ,IPR & biodiversity; IPR development process, role of WIPO and WTO in IPR establishments, common rules of IPR practices, types and features of IPR agreement, functions of UNESCO in IPR maintenance.

UNITV PATENTS **9**

Patents – objectives and benefits of patent, concept, features of patent, inventive steps, specifications, types of patent application; patenting process - patent filling, examination of patent, grant of patent, revocation; equitable assignments; Licenses, licensing of patents; patent agents, registration of patent agents.

TOTAL:45PERIODS

COURSEOUTCOMES

Uponcompletionofthecourse,thestudentcan
CO1:Describedifferent typesofresearch;identify,reviewanddefinetheresearchproblem
CO2:Selectsuitabledesignofexperiments;describetypesofdataandthetoolsforcollectionof data
CO3:Explaintheprocessofdataanalysis;interpretandpresenttheresultinsuitableform CO4:
Explain about Intellectual property rights, types and procedures
CO5:Executepatentfilingandlicensing

REFERENCES:

1. CooperDonaldR,SchindlerPamelaSandSharmaJK,“BusinessResearchMethods”,Tata McGraw Hill Education, 11e (2016).
2. SoumitroBanerjee, “Researchmethodologyfornaturalsciences”,IIScPress,Kolkata,2022,
3. CatherineJ.Holland,“Intellectualproperty:Patents,Trademarks,Copyrights,TradeSecrets”, Entrepreneur Press, 2015.
4. DavidHunt,LongNguyen,MatthewRodgers,“Patentsearching:tools&techniques”,Wiley, 2007.
5. TheInstituteofCompanySecretariesofIndia,StatutorybodyunderanActofparliament, “Professional Programme Intellectual Property Rights, Law and practice”, September 2015.

23VDP102 **DIGITALCMOSVLSIDESIGN**

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UNITI MOSTRANSISTORPRINCIPLESANDCMOS INVERTER12

MOSFETTransistorCharacteristicunderStaticandDynamicConditions,MOSTransistorSecondary Effects, Fabrication Process, Process variations, MOS device Modeling, CMOS Inverter-Static Characteristic, Dynamic Characteristic, Power, Energy, and Energy Delay parameters, Scaling Principles, Stick diagram and Layout diagrams.

UNIT II COMBINATIONALLOGICCIRCUITS 9

Static CMOS design, Different styles of logic circuits, Logical effort of complex gates, Static and Dynamic properties of complex gates, Interconnect Delay, Dynamic Logic Gates.

UNIT III SEQUENTIALLOGICCIRCUITS 9

StaticLatchesandRegisters,DynamicLatchesandRegisters,TimingIssues,Pipelines,Nonbistable Sequential Circuits.

UNIT IV ARITHMETICBUILDINGBLOCKSANDTESTING 9

Datapathcircuits,ArchitecturesforAdders,Accumulators,Multipliers,BarrelShifters,SpeedandArea Tradeoffs, Need for testing -Manufacturing test – Design for testability

UNITV MEMORY ARCHITECTURES 6

Memory Architectures and Memory control circuits : Read-Only Memories, ROM cells, Read- write memories (RAM), 6 SRAM cell, 3T DRAM and 1T DRAM Design, Sense amplifiers, CAM design.

COURSEOUTCOMES:

CO1: Tobeabletousemathematicalmethodsandcircuitanalysismodelsinanalysisof CMOSdigital circuits

CO2:Tobeabletocreatemodelsofmoderatelysized staticCMOScombinationalcircuitsthatrealize specifieddigitalfunctionsandtooptimizecombinationalcircuitdelayusingRCdelaymodelsand logical effort

CO3:Tobeabletodesignsequentiallogicatthetransistorlevelandcomparethetradeoffsof sequencing elements including flip-flops, transparent latches

CO4:Tobeabletolearndesignmethodologyofarithmeticbuildingblocks

CO5:TobeabletodesignfunctionalunitsincludingROMandSRAM

REFERENCES:

1. JanRabaey,AnanthaChandrakasan,BNikolic,“DigitalIntegratedCircuits:ADesign Perspective”, Prentice Hall of India, 2nd Edition, May 2016,
2. N.Weste,K.Eshraghian,“PrinciplesofCMOSVLSIDesign”,AddisonWesley,2nd Edition, 2015
3. MJSmith,“ApplicationSpecificIntegratedCircuits”,AddisonWesley,January2015.
4. Sung-MoKang&YusufLeblebici,“CMOSDigitalIntegratedCircuitsAnalysisandDesign”, McGraw-Hill, December 2016.
5. BasicVLSIdesign“DouglasA.pucknellandKamranEshraghian”,PrenticeHallPublications, 2017

23VDP103 ANALOGINTEGRATEDCIRCUITDESIGN

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UNITI SINGLESTAGEANDITSFREQUENCYRESPONSE 9

Basic MOS physics and equivalent circuits and models, CS, CG and Source Follower, Miller effect, association of poles with nodes, Dominant-Pole approximation, Upper Cutoff frequency-zero-value time constant method, UGF-short circuit time constant method, frequency response of CS, CG and source follower.

UNITII VOLTAGEANDCURRENTREFERENCES 6

Current sinks and sources, Current mirrors, Wilson current source, Widlar current source, Cascode current source, Design of high swing Cascode sink, current amplifiers,Sooch Current Mirror,

UNIT III DIFFERENTIALAMPLIFIERSANDNOISECHARACTERISTICSOFAMPLIFIERS 12

Differential amplifier with active load, Design of differential telescopic Cascode and folded Cascode configurationswithactiveload,tomeetspecifiedSR,gain,BW,ICMRandpowerdissipation,voltage swing, High gain amplifier, structures., Two-stage OpAmps, Input range limitations, Gain boosting, slewrate,powersupplyrejection,thermalnoise,flickernoise,Statisticalcharacteristicsofnoise,noise in single stage amplifiers, noise in differential amplifiers.

UNITIII NEGATIVEFEEDBACKAMPLIFIERSANDVOLTAGEREFERENCES 9

Propertiesandtypesofnegativefeedbackcircuits,effectofloadinginfeedbacknetworks, return-ratio analysis, operational amplifier performance parameters, One-stage Op Amps, Supply independent biasing, temperature independent references, PTAT and CTAT current generation, Constant-Gm Biasing.

UNIT IV STABILITY AND FREQUENCY COMPENSATION OF TWO STAGE OPERATIONALAMPLIFIER 9

Analysis of two stage Op Amp- two stage Op Amp single stage CMOS CS as second stageand using Cascode second stage, multiple pole system,Phase Margin, Frequency Compensation, and CompensationoftwostageOpAmps,SlewingintwostageOpAmps,Othercompensationtechniques.

UNIT V STABILITY AND FREQUENCY COMPENSATION OF TWO STAGE OPERATIONALAMPLIFIER 9

Analysis of two stage Op Amp- two stage Op Amp single stage CMOS CS as second stageand using Cascode second stage, multiple systems,Phase Margin, Frequency Compensation, and CompensationoftwostageOpAmps,SlewingintwostageOpAmps,Othercompensationtechniques.

TOTAL:45PERIODS

PRACTICALEXERCISES:

1. ExtractionofprocessparametersofCMOSprocessTransistors
a. PlotIDvs.VGSatdifferentdrainvoltagesfornMOS,PMOS.
b. PlotIDvs.VGSatparticulardrainvoltage(low)forNMOS,PMOSanddetermineVt.
c. PlotlogIDvs.VGSatparticulargatevoltage(high)forNMOS,PMOSand determine IOFF and sub-threshold slope.

d. PlotIDvs.VDSatdifferentgatevoltagesforNMOS,PMOSanddetermineChannel length modulation factor.

2. ConsiderasimpleCSamplifierwithactiveload,withNMOStransistorasdriverand PMOS transistor as load.

a. Calculateinputbiasvoltageforagivenbiascurrent.

b. Usespiceandobtainthebiascurrent.Comparewiththetheoreticalvalue

c. Determinesmallsignalvoltagegain,-3dBBWandGBWoftheamplifierusingsmallsignalanalysisin spice, considering load capacitance.

d. Plotstepresponseoftheamplifierwithaspecificinputpulseamplitude.Derivetimeconstantofthe outputandcompareitwiththetimeconstantresultedfrom-3dB BW.

e. Usespicetodetermineinputvoltagerangeoftheamplifier.

3. RealizelayoutandperformpostlayoutsimulationoftheCSamplifierrealizedinEx.No.2

4. Designadifferential amplifierwithresistiveloadusingtransistorsfromCMOSprocesslibrarythat meets a given specification for the following parameter

a. PerformDCanalysisanddetermineinputcommonmoderangeandcomparewiththetheoretical values.

b. Performtimedomainsimulationandverifylowfrequencygain.

c. PerformACanalysisandverifylow-frequencyvoltagegainandunitygainBW (fu)

5. StabilityAnalysisofTwostageOpAmp

a. PerformDCanalysisanddetermineinputcommonmoderangeandcomparewiththetheoretical values.

b. Performtimedomainsimulationandverifylowfrequencygain.

c. PerformACanalysisandverifylow-frequencyvoltagegainandunitygainBW (fu)

TOTAL:60PERIODS

COURSEOUTCOMES:

CO1:Abilitytodesignamplifierstomeetuserspecifications
CO2: Ability to analyse the frequency and noise performance of amplifiers
CO3:AbilitytodesignandanalysenegativefeedbackamplifiersandopAmps**CO4**:
Ability to analyse stability aspects of two stage opAmps
CO5:Abilitytodesignandusecurrentmirrors,currentsourcesusingMOSdevices

REFERENCES:

1. BehzadRazavi,"DesignofAnalogCMOSIntegratedCircuits",TataMcGrawHill,2nd Editio n, 2016.
2. WilleyM.C.Sansen,"AnalogDesignEssentials",Springer,March2015.
3. Grebene,"BipolarandMOSAnalogIntegratedcircuitdesign",JohnWiley&sons, Inc.,203.
4. PhillipE.Allen,DouglasR.Holberg,"CMOSAnalogCircuitDesign",Oxford University Press, 3rdOctober 2016.
5. Recordedlectureavailableathttp://www.ee.iitm.ac.in/~ani/ee5390/index.html
6. JacobBaker"CMOS:CircuitDesign,Layout,andSimulation,ThirdEdition",WileyIEEE Press, 4thEdition,August 2019.
7. AnalysisandDesignofAnalogIntegratedCircuits,6thEdition, PaulR.Gray,PaulJ.Hurst,Stephen H. Lewis,Robert G. Meyer, Wiley Publications, 2024

23VDP104	VLSIDIGITALSIGNALPROCESSING	L	TP	C
		3	00	3

UNITI INTRODUCTIONTODSPSYSTEMS,PIPELININGANDPARALLEL PROCESSING OF FIR FILTERS 9

Introductionto DSP systems –Typical DSP algorithms, Data flowand Dependence graphs - critical path,Loopbound,iterationbound,Longestpathmatrixalgorithm,Pipelining andParallelprocessing of FIR filters, Pipelining and Parallel processing for low power.

UNITII RETIMING,ALGORITHMICSTRENGTHREDUCTION 9

Retiming – definitions and properties, Unfolding – an algorithm for unfolding, propertiesof unfolding, sampleperiodreduction andparallelprocessing application, Algorithmic strength reduction in filters andtransforms–2-parallelFIRfilter,2-parallelfastFIRfilter,DCTarchitecture,rank-orderfilters, Odd-Evenmerge-sortarchitecture,parallelrank-orderfilters.

UNITIII FASTCONVOLUTION,PIPELININGANDPARALLEL PROCESSINGOFIIRFILTERS 9

Fastconvolution–Cook-Toomalgorithm,modifiedCook-Toomalgorithm,Pipelinedandparallel recursive filters – Look-Ahead pipelining in first-order IIR filters, Look-Ahead pipelining with power-of-2decomposition,Clusteredlook-aheadpipelining,ParallelprocessingofIIRfilters,combined pipeliningandparallelprocessingofIIRfilters, Design and analysis of IIR filter.

UNITIV BIT-LEVELARITHMETICARCHITECTURES 9

Bit-level arithmetic architectures – parallel multipliers with sign extension, parallel carry ripple and carry-savemultipliers, Designof Lyon‟s bit-serialmultipliers using Horner‟s rule, bit-serialFIRfilter, CSD representation, CSD multiplication using Horner‟s rule for precision improvement, Distributed Arithmetic fundamentals and FIR filters.

UNITV NUMERICALSTRENGTHREDUCTION,SYNCHRONOUS, WAVEANDASYNCHRONOUSPIPELINING 9

Numericalstrengthreduction–sub expressionelimination, multiple constant multiplication, iterative matching, synchronous pipelining and clocking styles, clock skew in edge-triggered single phase clocking, two-phase clocking, wave pipelining. Asynchronous pipelining bundled data versus dual rail protocol.

TOTAL:45PERIODS

COURSE OUTCOMES:

CO1:Abilitytodeterminetheparametersinfluencingtheefficiencyof DSParchitecturesandapply pipelining and parallel processing techniques to alter FIR structures for efficiency

CO2:Abilitytoanalyseandmodifythedesignequationsleadingtoefficient DSParchitecturesfor transforms
CO3:Abilitytospeedupconvolutionprocessanddevelopfastandareaefficient IIRstructures
CO4:Abilitytodevelopfastandareaefficientmultiplier architectures
CO5:Abilitytoreducemultiplicationsandbuildfasthardwarefor synchronous digitalsystems

REFERENCES

1. KeshabK.Parhi,"VLSIDigitalSignalProcessingSystems,Designandimplementation", Wiley, Interscience, 2015.
2. U. Meyer- Baese,"DigitalSignalProcessingwithFieldProgrammableGateArrays", Springer,4thEdition,June2015.

23VDP105 HARDWAREDESCRIPTIONLANGUAGESFORRTLDESIGNS L T PC
3 0 45

UNITI BASICSOFVHDL 6

Entitydeclaration- Architecturebody-CreatingI/OPortsforDifferentDataTypes-Signal,Constant and variable - VHDLoperators - Assignment operators, Logical operators, arithmetic operators and shift operators – Generic statement – VHDL statements - concurrent signal assignment statements and sequential statements–Packages,Components,Functions andProcedures –Testbench.

UNITII BASICSOFVERILOG 6

Module–Moduleports-Verilogoperators–Datatypes–net,regdeclarations-Constantsand Arrays–Module parameters -Continuousand ProceduralAssign statements –Conditional Expressions – Sequential statements - blocking and non-blocking assignments - Primitive instantiations – Module instantiations – Compiler directives – Test bench.

UNITIII HDLSYSTEMDESIGN 6

CombinationalCircuit Design – Adder, Subtractor,Comparator, Priorityencoder, Mux/Demux, Code converters, Array multiplier – Sequential circuit design – Latch, Flip flops, Registers, Shift registers, Counters, Sequential multiplier, State machine designs

UNITIV DESIGNCONSIDERATIONS &VERIFICATION 6

Timing Parameters – Metastability – Positive and Negative Clock skew – Setup slack and Hold slack-Clock latency – Area, Speed and Power requirements, Testing and verification.

UNITV INTRODUCTIONTORIPPLEANDPERLLANGUAGE 6

APipelinedMultiplierAccumulator–ALUDesign–SingleportandDualportMemorydesign– Design of DSP modules and MAC unit – IP cores: creation and usage.

TOTAL:45PERIODS

LABEXPERIMENTS:

1. HDLrealizationandtiminganalysisof
   - Combinationalcircuitsnamely8:1Mux/Demux,FullAdder,8-bitMagnitude comparator, Encoder/decoder, Priority encoder.
   - SequentialcircuitsnamelyD-FF,Shiftregisters(SISO,SIPO,PISO,bidirectional), Synchronous Counters.
2. FPGAimplementationofPCIBus&arbiter.
3. RealizationofUART/USARTimplementationinHDLanddesignvalidationusingtest vector generation.
4. FPGArealizationofsingleportSRAMandcapturingthesignalinDSO.
5. BackannotationandtiminganalysisofArithmeticcircuitslikeserialadder/subtractor, parallel adder/subtractor, serial/parallel multiplier.
6. RealizationofDiscreteFouriertransform/FastFourierTransformalgorithmin HDL/RTL and observing the spectrum in simulation.
7. DesignandimplementFIRandIIRfilters
8. Designandimplementadaptivefilters

TOTAL:60PERIODS

COURSEOUTCOMES:

Attheendofthiscoursestudentswillbeableto

CO1:UsethebasicdatatypesandoperatorsinVerilog/VHDL

CO2:DesignarithmeticmodulesusingVerilog and VHDL

CO3:AnalysepowerdissipationandpropagationdelayoftheRTLmodules

CO4::AbilitytoValidatethedesigninFPGAstartingfromdesignentrytobackannotation.

CO5:DesignmacromodulessuchasALU,MAC,etc

REFERENCES:

1. PongP.Chu,RTLHardwareDesignusingVHDLCodingforEfficiency,Portability,and Scalability, Wiley Interscience Publication, 2015, ISBN-13: 978-0-471-72092-8.
2. MingBoLin,DigitalSystemDesignsandPractices-usingVerilogHDLandFPGAs,Wiley India Pvt. Ltd., 2015, Reprint 2012.
3. PeterJ.Ashenden,TheDesigner'sGuidetoVHDL,ThirdEdition,Elsevier,2015.ISBN:978-0-12-088785-9.
4. PeterJ.Ashenden,DigitalDesign –AnEmbeddedSystemsApproachusingVerilog,Elsevier Inc., 2015, ISBN: 978-0-12-369527-7.
5. VaibbhavTaraate,ASICDesignandSynthesis-RTLDesignusingVerilog,Springer,2021.

23VDP201 DESIGNFORVERIFICATIONUSINGUVM LTP C 3003

COURSEOBJECTIVES:

- ToprovidethestudentscompleteunderstandingonUVMtesting
- TobecomeproficientatUVMverification,
- ToprovideanexperienceonselfcheckingUVMtestbenches

UNITI INTRODUCTION 9

Overview- The Typical UVM Testbench Architecture- The UVM Class Library-Transaction-Level Modeling (TLM) -Overview- TLM, TLM-1, and TLM-2.0 -TLM-1 Implementation- TLM-2.0 Implementation

UNITII DEVELOPINGREUSABLEVERIFICATIONCOMPONENTS 9

Modeling Data Items for Generation- Transaction-Level Components - Creating the Driver - CreatingtheSequencer-ConnectingtheDriverandSequencer-CreatingtheMonitor-Instantiating Components- Creating the Agent - Creating the Environment -Enabling Scenario Creation - Managing of Test-Implementing Checks and Coverage

UNITIII UVMUSINGVERIFICATIONCOMPONENTS 9

CreatingaTop-LevelEnvironment- InstantiatingVerificationComponents- CreatingTestClasses -Verification Component Configuration - Creating and Selecting a User-Defined Test - Creating MeaningfulTests-VirtualSequences-CheckingforDUTCorrectness-Scoreboards-Implementing a Coverage Model

UNITIV UVMUSING THEREGISTERLAYERCLASSES 9

UsingTheRegisterLayerClasses-Back-DoorAccess-SpecialRegisters-IntegratingaRegister-ModelinaVerificationEnvironment-IntegratingaRegisterModel-RandomizingFieldValues-Pre-Defined Sequences

UNITV ASSIGNMENTINTESTBENCHES 9

Assignment,APB:Protocol,TestbenchArchitecture,DriverandSequencer,Monitor, Agentand Env;CreatingSequences,BuildingTest,DesignandTestingofTopModule.

TOTAL:45PERIODS

COURSEOUTCOMES:

At the end of the course, students will be able to

CO1:understandthebasicconceptsoftwomethodologiesUVM

CO2:build actual verification components.

CO3:generatetheregister layerclasses.

CO4:codetestbenchesusingUVM.

CO5:understandadvancedperipheralbustestbenches.

REFERENCES

1. TheUVMPrimer,An Introduction to theUniversal VerificationMethodology,Ray Salemi, 2015.
2. SystemVerilogforVerification:AGuidetoLearningtheTestbenchLanguageFeatures, Chris Spear, Greg Tumbush, 3rd edition, 2016.
3. https://www.udemy.com/learn-ovm-UVM/

4.http://www.testbench.in/ut_00_index.html

5. http://www.testbench.in/ot_00_index.html
6 https://www.accellera.org/images/downloads/standards/UVM/UVM_users_guide_1.2.pdf

23VDP202	LOWPOWERVLSIDESIGN	L	TP	C
		3	04	5

UNITI POWERDISSIPATIONINCMOS 9

Hierarchyoflimitsofpower-Sourcesofpowerconsumption-PhysicsofpowerdissipationinCMOS FET devices – Basic principle of low power design.

UNITII POWEROPTIMIZATION 9

Logic level power optimization – Circuit level low power design – Gate level low power design – Architecturelevellowpower design – VLSI subsystem designof adders, multipliers, PLL, low power design.

UNITIII DESIGNOFLOWPOWERCMOSCIRCUITS 9

Computer arithmetic techniques for low power system – reducing power consumption in combinational logic, sequential logic, memories – low power clock – Advanced techniques – Special techniques, Adiabatic techniques – Physical design, Floor planning, placement and routing.

UNITIV POWERESTIMATION 9

Power Estimation techniques, circuit level, gate level, architecture level, behavioral level, – logic power estimation – Simulation power analysis -Probabilistic power analysis.

UNITV SYNTHESISANDSOFTWAREDESIGNFORLOWPOWER 9

Synthesisforlowpower-Behavioralleveltransform-Algorithmsforlowpower-softwaredesignfor low power.

TOTAL:45PERIODS

LISTOFEXPERIMENTS:

1. CMOSinverterdesignand performanceanalysis
   - PlotVTCcurveforCMOSinverterandthereonplotdVoutvs.dVinanddetermine transition voltage and gain. Calculate VIL, VIH, NMH, NML for the inverter.
   - PlotVTCforCMOSinverterwithvaryingVDD.
   - PlotVTCforCMOSinverterwithvaryingdeviceratio.
   - Redesigntheinverterforsymmetricaltransientresponseandminimumpropagation delay to for a given load capacitance. Perform transient analysis of CMOS inverter with no load and with load and determine tpHL, tpLH,
   - PerformACanalysisofCMOSinverterwithfanout0andfanout1.
2. Usespicetobuildathreestageandfivestageringoscillatorcircuitandcompareits frequencies. Use FFT and verify the amplitude and frequency componentsin the spectrum
3. UseLayouteditor.
   - DrawlayoutofaminimumsizeinverterusingtransistorfromCMOSprocesslibrary. Use Metal 1 as interconnect line between inverters.
   - RunDRC,LVSandRCextraction.MakesurethereisnoDRCerror.
   - Extractthenetlist.Useextractednetlistandobtain$t_{PHL}$$t_{PLH}$fortheinverterusing Spice.
   - Useaspecificinterconnectlengthandconnectandconnectthreeinvertersina chain. Extract the new netlist and obtain $t_{PHL}$and $t_{PLH}$of the middle inverter.

- Comparenewvaluesofdelaytimeswithcorrespondingvaluesobtainedinpart‘c’.

4. Analogcircuitscasestudies-SchematicentrytoGDSIIlayout
5. Digitallogicscasestudies-RTLDesignentrytoGDSIIlayout
6. Verificationofpowerreductiontechniquesbyclockgating,powergatingandfactorization.

TOTAL:60PERIODS

COURSEOUTCOMES:

CO1:AbilitytofindthepowerdissipationofMOScircuits
CO2:DesignandanalysevariousMOSlogiccircuits
CO3:Applylowpowertechniquesforlowpowerdissipation
CO4:AbletoestimatethepowerdissipationofICs
CO5:Abilitytodevelop algorithmtoreducepowerdissipationbysoftware.

REFERENCES:

1. KaushikRoyandS.C.Prasad,“LowpowerCMOSVLSIcircuitdesign”,Wiley,January2019.
2. J.B.KuloandJ.HLou,“LowvoltageCMOSVLSICircuits”,Wiley2019
3. A.P.ChandrasekaranandR.W.Broadersen,“Low power digitalCMOSdesign”,Kluwer, October 2012.
4. GaryYeap,“PracticallowpowerdigitalVLSIdesign”,Kluwer,October2012.
5. AbdelatifBelaouar,Mohamed.I.Elmasry,“LowpowerdigitalVLSIdesign”,Kluwer, September 2012.
6. JamesB.Kulo,Shih-ChiaLin,“LowvoltageSOICMOSVLSIdevicesandCircuits”,John Wiley and sons,inc. 2021.
7. J.Rabaey,“Low PowerDesignEssentials(IntegratedCircuitsand Systems)”,Springer, 2020.

23VDP203 CADFORVLSIDESIGN LTP C
3003

COURSEOBJECTIVES:

- tointroducetheVLSIdesignmethodologiesanddesignmethods.
- tointroducedatastructuresandalgorithmsrequiredforVLSIdesign.
- tostudyalgorithmsforpartitioningandplacement.
- tostudyalgorithmsforfloorplanningandrouting.
- tostudyalgorithmsformodelling,simulation andsynthesis.

UNITI INTRODUCTION 9

Introduction toVLSIDesign Methodologies -VLSIDesignCycle-NewTrendsinVLSIDesignCycle - Physical Design Cycle - New Trends in Physical Design Cycle - Design Styles - Reviewof VLSI Design Automation Tools

UNITII DATASTRUCTURESANDBASICALGORITHMS 9

Introduction to Data Structures and Algorithms - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable Problems - General Purpose Methods for Combinatorial Optimization.

UNITIII ALGORITHMSFORPARTITIONINGANDPLACEMENT 9

LayoutCompaction-ProblemFormulation-AlgorithmsforConstraintGraphCompaction-Partitioning - Placement - Placement Algorithms.

UNITIV ALGORITHMSFORFLOORPLANNINGANDROUTING 9

Floorplanning-ProblemFormulation-FloorplanningAlgorithms-Routing-AreaRouting- Global Routing -Detailed Routing.

UNITV MODELLING, SIMULATION ANDSYNTHESIS 9

Simulation-GateLevelModelingandSimulation-LogicSynthesisandVerification-Binary Decision Diagrams - High Level Synthesis.

TOTAL:45 PERIODS

COURSEOUTCOMES:

Attheendofthiscourse,thestudentsshouldbeableto:

CO1:usevariousVLSIdesignmethodologies

CO2:understanddifferentdatastructuresandalgorithmsrequiredforVLSIdesign.

CO3:developalgorithmsfor partitioningandplacement.

CO4:developalgorithmsforfloorplanningandrouting.

CO5:designalgorithmsformodelling,simulationandsynthesis.

REFERENCES

1.SabihH.Gerez,"AlgorithmsforVLSIDesignAutomation",SecondEdition,Wiley-India, 2017.

2.Naveeda.Sherwani,"AlgorithmsforVLSIPhysicalDesignAutomation",3rdEdition, Springer,2017.

3.CharlesJ.Alpert,DineshP.MehtaandSachinSSapatnekar,"HandbookofAlgorithmsfor PhysicalDesignAutomation,CRCPress,1stEdition,2.

4.N.a.Sherwani,"AlgorithmsforVLSIPhysicalDesignAutomation",KluwerAcademic Publishers, 2015.

23VDP221 **VERIFICATIONUSINGUVMLABORATORY** **LTP C 0042**

COURSEOBJECTIVES:

- tohelptheengineerstodesignthesystemwithverilogandsystemVerilog
- CompleteunderstandingofVerilogHardwareDescriptionLanguage
- topracticeforwritingsynthesizableRTLmodelsthatworkcorrectlyinbothsimulationand synthesis.

LISTOFEXPERIMENTS

1. SimulateasimpleUVMtestbenchandDUT
2. Examiningthe UVMtestbench
3. Designandsimulatesequenceitemsandsequence
4. DesignandsimulateaUVMdriverandsequencer
5. DesignandsimulatingUVMmonitorandagent
6. Design, simulateandexaminecoverage
7. DesignandsimulateaUVMscoreboardand environment, and verifying the outputsofa (faulty) DUT
8. Designandsimulateatestthatrunsmultiplesequence
9. DesignandsimulateaconfigurableUVMtestenvironment

TOTAL:45PERIODS

COURSEOUTCOMES:

Onsuccessfulcompletionofthiscourse,studentswillbeableto

CO1:understandthefeaturesandcapabilitiesoftheUVMclasslibraryforsystemVerilog

CO2:combinemultipleUVCsintoacompleteverificationenvironment

CO3:create and configure reusable, scalable, and robust UVM verification components (UVCs)

CO4: create a UVM testbench structure using the UVM library base classes and the UVM factory

CO5:developaregistermodelforyourDUTandusethemodelforinitializationandaccessingDUT Registers

23VDP222 TERMPAPERWRITINGANDSEMINAR LTPC
0042

In this course, students will develop their scientific and technical reading and writing skills that they need to understand and construct research articles. A term paper requires a student to obtain informationfrom a varietyof sources (i.e., Journals, dictionaries, reference books) and then place it in logically developed ideas. The work involves the following steps:

1. Selectingasubject,narrowingthesubjectintoatopic
2. Statinganobjective.
3. Collectingtherelevantbibliography(atleast15journalpapers)
4. Preparingaworkingoutline.
5. Studyingthepapersandunderstandingtheauthorscontributionsandcriticallyanalysing
6. eachpaper.
7. Preparingaworkingoutline
8. Linkingthepapersandpreparingadraftofthepaper.
9. Preparingconclusionsbasedonthereadingofallthepapers.
10. WritingtheFinalPaperandgivingfinalPresentation

Pleasekeepafilewheretheworkcarriedoutbyyouismaintained. Activities to be carried out

Activity	Instructions	Submission week	Evaluation
Selectionofarea ofinterestand Topic Statingan Objective	Youarerequestedtoselectanareaofinterest, topic and state an objective	2nd week	**3%** Basedonclarityof thought, current relevance and clarity inwriting
Collecting Informationabout yourarea& topic	1. List1SpecialInterestGroupsor professional society 2. List2 journals 3. List2conferences,symposiaorworkshops 4. List1thesistitle 5. List3webpresences(mailinglists, forums, news sites) 6. List3authorswhopublishregularlyinyourarea 7. Attachacallforpapers(CFP)fromyour area.	3rd week	**3%** (the selected informationmustbe areaspecificandof international and national standard)

Collection of Journalpapersin the topic in the context of the objective-collect 20 & then filter	• You have to provide a complete listof references you will be using- Based on your objective -Search various digital libraries and Google Scholar • Whenpickingpaperstoread-tryto: • Pick papers that are related to each other in some ways and/or that are in the same field so that you can write a meaningful survey out of them, • Favour papers from well-known journals and conferences, • Favour “first” or “foundational”papers in the field (as indicated in other people’s survey paper), • Favourmorerecentpapers, • Picka recentsurvey ofthe fieldsoyou can quickly gain an overview, • Findrelationshipswithrespecttoeach otherandtoyourtopicarea (classificationscheme/categorization) • Mark in the hard copy of papers whether complete work or section/sections of the paper are being considered	4thweek	**6%** (the list of standardpapers and reason for selection)
Reading and notesforfirst5 papers	• ReadingPaperProcess • For each paper form a Table answering the following questions: • Whatisthemaintopicofthearticle? • Whatwas/werethemainissue(s)the author said they want to discuss? • Whydidtheauthorclaimitwas important? • Howdoestheworkbuildonother’s work, in the author’s opinion? • Whatsimplifyingassumptionsdoesthe author claim to be making? • Whatdidtheauthordo? • Howdidtheauthorclaimtheywere going to evaluate their work and compare it to others? • Whatdidtheauthorsaywerethe limitations of their research?	5thweek	**8%** (the table given should indicate your understanding of thepaperandthe evaluation is based on your conclusionsabout each paper)

	• Whatdidtheauthorsaywerethe important directions for future research? • Concludewithlimitations/issuesnot addressed by the paper (from the perspective of your survey)		
Reading and notesfornext5 papers	RepeatReadingPaperProcess	6thweek	**8%**(the table given shouldindicateyour understandingofthe paper and the evaluation is based onyourconclusions abouteachpaper)
Reading and notesforfinal5 papers	RepeatReadingPaperProcess	7thweek	**8%**(the table given shouldindicateyour understandingofthe paper and the evaluation is based onyourconclusions abouteachpaper)
Draftoutline1 and Linking papers	PrepareadraftOutline,yoursurveygoals, alongwithaclassification/categorization diagram	8thweek	**8%**(thiscomponentwill beevaluatedbased on the linking and classificationamong thepapers)
Abstract	Prepareadraftabstractandgivea presentation	9thweek	**6%**(Clarity,purposeand conclusion) **6%**Presentation& VivaVoce
Introduction Background	Writeanintroductionandbackground Sections	10thweek	**5%**(clarity)
Sectionsofthe paper	Write the sections of your paper based on the classification / categorization diagram in keeping with the goals of your survey	11thweek	**10%**(thiscomponentwil l beevaluatedbased on the linking and classificationamongthe papers)
Yourconclusions	Writeyourconclusionsandfuturework	12thweek	**5%**(conclusions – clarityandyour ideas)
FinalDraft	Completethefinaldraftofyourpaper	13thweek	**10%**(formatting, English,Clarityand linking) **4%**PlagiarismCheck report
Seminar	Abrief15slidesonyourpaper	14th&15th week	**10%**(basedon presentationan d Viva-voce)

TOTAL:30PERIODS

23VDP321	PROJECT WORK PHASE-1	L	T	P	C
		0	0	12	6

COURSE DESCRIPTION:

This course provides an opportunity for students to apply their engineering knowledge to solve real-world problems through project-based learning. Students, working in groups with maximum of 4 under faculty supervision, undertake a comprehensive project addressing an approved topic. The course focuses on fostering collaboration, research, and practical skills, culminating in a detailed Phase 1 project report and oral presentations. Regular reviews ensure consistent progress and adherence to academic standards.

COURSE OBJECTIVES:

Encourage students to apply theoretical knowledge to practical engineering problems.
Develop collaborative and project management skills through teamwork.
Train students in research methodology, technical documentation, and presentation skills.
Enhance students' ability to design, analyze, and evaluate solutions systematically.
Prepare students for real-world engineering challenges and multidisciplinary teamwork

PROJECT OUTLINE:

Week 1	Orientation and course overview. Formation of project teams and approval of topics by HoD.
Week 2	Initial meeting with supervisors. Define problem statement and objectives
Week 3	Literature review: Research methodologies and topic-specific studies.
Week 4	Zeroth Review.
Week 5	Refinement of literature review and identification of research gaps.
Week 6	Identification of Base Paper.
Week 7	First Review.
Week 8	Conceptual design discussions and brainstorming solutions.
Week 9	Narrowing done on the exact work.
Week 10	Completion of first stage of the Project.
Week 11	Development of detailed conceptual design and methodology.
Week 12	Incorporation of feedback and refinement of design and methodology.
Week 13	Second Review.
Week 14	Compilation of Phase 1 results, report writing, and presentation preparation.
Week 15	Final Viva Voce Presentations.

Individual meetings will be set up on a need's basis in conjunction with developing work

EVALUATION:

The progress of the project is evaluated based on a minimum of two reviews. The review committee may be constituted by the Head of the Department. A phase 1 project report is required to be submitted at the end of the semester. Evaluation is based on oral presentation and the phase 1 project report jointly by internal examiners constituted by the Head of the Department.

Evaluate how effectively the project is structured and communicated in both oral presentations and written texts, emphasizing logical flow and coherence.

Evaluate the relevance and innovation of practical resources or prototypes developed, focusing on their potential to support sustainability, innovation, and SDG-aligned goals.

Review the accuracy of English usage, including grammar, clarity, and coherence in oral and written communication, ensuring effective delivery of technical content.

COURSE OUTCOMES:

After completion of the course, the students will be able to:

CO1: Develop feasible solutions by analyzing complex engineering problems using foundational knowledge, mathematics, and science.

CO2: Survey literatures to identify gaps, define research questions, and propose designs and methods for solving engineering problems.

CO3: Make use of modern tools to check the feasibility of the solutions effectively.

CO4: Evaluate societal and environmental impacts of solutions while incorporating sustainability and ethical practices.

CO5: Combine in teams to plan, manage, and lead projects within professional and economic constraints.

23VDP421	PROJECT WORK PHASE-2	L	T	P	C
		0	0	24	12

COURSE DESCRIPTION:

Project Phase 2 is a continuation of Project Phase 1, focusing on implementing the proposed methodology through fabrication, simulation, or experimental validation. Students will refine their designs, validate test problems, and commission setups for final testing. This phase emphasizes hands-on application, calibration, and demonstration of results, culminating in a final presentation and report submission.

COURSE OBJECTIVES:

- Implement the proposed methodology to address engineering problems identified in Phase 1.
- Develop and fabricate prototypes or simulate solutions for the selected project integrating theoretical knowledge with practical application across hardware and software systems.
- Validate solutions through testing ensuring reliability and performance in both physical and virtual environments.
- Enhance problem-solving and critical thinking skills by troubleshooting and optimizing either experiment setups or software code to improve results.
- Prepare a research manuscript or applying for patent grant either for design or research.

PROJECT OUTLINE:

Week 1	Review of Phase 1 outcomes and refinement of proposed methodology.
Week 2	Material procurement/ software setup for simulation, and initiation of fabrication/simulation work.
Week 3	Intermediate fabrication/simulation work and initial testing or calibration, troubleshooting challenges.
Week 4	Second Review.
Week 5	Validation of test problem or refinement of prototype/simulation
Week 6	Optimisation of the test setup or solution trials, Data curation / uncertainty analysis
Week 7	Final testing of setup or simulation outcomes, Validation of Data
Week 8	Third Review
Week 9	Demonstration of the solution with high level of data accuracy and precision.
Week 10	Compilation of Phase 2 results, report writing, and presentation preparation.
Week 11	Preparing or publishing of research article/ Filing or Grant of Patent
Week 12	Final Viva Voce Presentations.

Individual meetings will be set up on a need's basis in conjunction with developing work

EVALUATION:

- The progress of the project is evaluated based on a minimum of two reviews. The review committee may be constituted by the Head of the Department. A project report is required at the end of the semester. The project work is evaluated based on oral presentation and the project report jointly by external and internal examiners constituted by the Head of the Department.
- Assess the depth of understanding demonstrated in the project's conceptualization and the ability to answer questions during public presentations.
- Publication of Research article in indexed journal or Patent award is necessary at the end of completion of the project.

COURSE OUTCOMES:

After completion of the course, the students will be able to:

CO1: Apply appropriate methodologies to implement solutions for complex engineering problems identified in phase -1 using hardware / software or both systems.

CO2: Develop existing functional prototypes or simulations models by integrating theoretical and practical knowledge.

CO3: Evaluate solutions ensuring compliance with design specifications.

CO4: Appraise the performance of solutions by refining designs or improving algorithms for enhanced outcomes.

CO5: Collaborate effectively with team members to plan, manage, and execute engineering projects adhering to ethical principles and professional standards.

23VDP041 **ASICDESIGN** **LTPC**
3003

COURSEOBJECTIVES:

- ToFocusontheSemi-CustomICDesignandintroducesthePrinciplesof DesignLogicCells, I/O Cells and Interconnect Architecture, with Equal Importance given to FPGA and ASIC styles.
- TodealwiththeentireFPGAandASICDesignFlowfromtheCircuitandLayoutDesignPoint of View

UNITI **INTRODUCTIONTO ASICS,CMOSLOGICANDASIC LIBRARYDESIGN** **9**

TypesofAsics-DesignFlow-CMOSTransistors-CombinationalLogicCell-SequentialLogicCell -DataPathLogicCell-TransistorsasResistors-TransistorParasiticCapacitance-LogicalEffort.

UNITII **PROGRAMMABLEASICS,PROGRAMMABLEASICLOGIC CELLSAND PROGRAMMABLEASICI/OCELLS** **9**

AntiFuse- StaticRam - EPROMandEEPROMTechnology - ACTEL ACT- XilinxLCA –ALTERA FLEX - ALTERA MAX DC & AC Inputs and Outputs - Clock & Power Inputs - Xilinx I/O Blocks.

UNITIII **PROGRAMMABLEASICARCHITECTURE** **9**

Architecture and Configuration ofARTIX / Cyclone and KINTEXUltra Scale /STRATIXFPGA – Micro-Blaze / NIOS Based Embedded Systems –Signal ProbingTechniques.

UNITIV **LOGICSYNTHESIS,PLACEMENTANDROUTING** **9**

Logic Synthesis - Floor Planning Goals and Objectives, Measurement of Delay in Floor Planning, Floor Planning Tools, I/O and Power Planning, Clock Planning, Placement Algorithms. Routing: Global Routing, Detailed Routing, Special Routing.

UNITV **SYSTEM-ON-CHIPDESIGN** **9**

SoC Design Flow, Platform-Based and IP Based SoC Designs, Basic Concepts of Bus-Based Communication Architectures, High Performance Filters using Delta-Sigma Modulators.Case Studies: Digital Camera, SDRAM, High Speed Data standards.

TOTAL:45PERIODS

COURSEOUTCOMES:

Attheendofthiscourse,thestudentswillbe

CO1:able to applyLogicalEffortTechniqueforpredictingDelay,DelayMinimization and FPGA Architectures

CO2:abletoDesignLogicCellsandI/OCells

CO3:abletoanalyzethevariousresourcesofrecentFPGAs

CO4:abletouseAlgorithmsforFloorPlanningandPlacementofCellsandtoApplyRouting Algorithms for Optimization of Length and Speed.

CO5:abletoanalyzeHigh PerformanceAlgorithmsAvailablefor ASICs

REFERENCES

1.M.J.S.Smith,"ApplicationSpecificIntegratedCircuits",Pearson,2015.

2.SteveKilts,“AdvancedFPGADesign,”WileyInter-Science,2015

3.RogerWoods, John Mcallister, Dr. Ying Yi, Gaye Lightbod, “FPGA-Based Implementation of Signal Processing Systems”, Wiley, 2016.

23VDP042 EMBEDDEDSYSTEMDESIGN LTPC
3003

COURSEOBJECTIVES:

- Tounderstandthedesignchallengesinembeddedsystems.
- Toprogram theApplicationSpecificInstructionSet Processors.
- Tounderstandthebusstructuresandprotocols.
- Tomodelprocessesusingastate-machinemodel.
- Todesignarealtimeembeddedsystem.

UNITI EMBEDDEDSYSTEMOVERVIEW 9

Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Components, Optimizing Custom Single-Purpose Processors.

UNITII GENERALANDSINGLEPURPOSEPROCESSOR 9

Basic Architecture, Pipelining, Superscalar and VLIW Architectures, Programmer's View, Development Environment, Application-Specific Instruction-Set Processors (ASIPS) Microcontrollers, Timers, Counters and Watchdog Timer, UART, LCD Controllers and Analog-to-Digital Converters, Memory Concepts.

UNITIII BUSSTRUCTURES 9

BasicProtocolConcepts,Microprocessor Interfacing– I/OAddressing,PortandBus -basedI/O, Arbitration,SerialProtocols,I2C,CANandUSB,ParallelProtocols -PCIandARMbus,Wireless Protocols– IRDA, Advanced Bluetooth low energy technologies, IEEE 802.11be

UNITIV STATEMACHINEANDCONCURRENTPROCESSMODELS 9

BasicStateMachineModel,Finite-StateMachinewithDatapathModel,CapturingStateMachine

in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, CommunicationamongProcesses,Synchronizationamongprocesses,RTOS– Systemdesign using RTOS.

UNITV SYSTEMDESIGN 9

Burglar alarm system-Design goals -Development strategy-Software development-Relevance to more complex designs- Need for emulation -Digital echo unit-Creating echo and reverb-Design requirements-Designing the codecs -The overall system design

SUGGESTEDACTIVITIES:

1:Domicrocontrollerbaseddesignexperiments.
2:Create program –statemodelsfordifferent embeddedapplications.
3:Designanddevelopembeddedsolutionsforrealworldproblems.

COURSEOUTCOMES:

CO1:Knowledgeofdifferent protocols
CO2: Applystatemachinetechniquesanddesignprocessmodels.
CO3:Applyknowledgeofembedded sotwaredevelopmenttoolsand RTOS
CO4:Applynetworkingprinciplesinembeddeddevices.
CO5: Designsuitableembeddedsystemsforrealworldapplications.

TOTAL:45PERIODS

REFERENCES:

1. FrankVahidandTonyGwargie,“EmbeddedSystemDesign”,JohnWiley&Sons,2019.
2. SteveHeath,“EmbeddedSystemDesign”,Elsevier,SecondEdition,2015.
3. BrucePowelDouglas,“RealTimeUML,SecondEdition:DevelopingEfficientObjectsfor EmbeddedSystems”,3rdEdition2016, PearsonEducation
4. DanielW.Lewis,“FundamentalsofEmbeddedSoftwarewhereCandAssemblyMeet”, PearsonEducation,2015
5. BrucePowelDouglas,“RealTimeUML;SecondEdition:DevelopingEfficientObjectsfor Embedded Systems”, 3rd Edition 2016 Pearson Education.

23VDP043 ELECTROMAGNETIC INTERFERENCEANDCOMPATIBILITY L TPC 3003

COURSEOBJECTIVES:

- Togainbroadconceptualunderstandingofthevariousaspectsofelectromagnetic(EM) interference and compatibility
- Todevelopatheoreticalunderstandingofelectromagneticshieldingeffectiveness
- TounderstandwaysofmitigatingEMIbyusingshielding,groundingandfiltering
- Tounderstandtheneedforstandardsandtoappreciatemeasurementmethods
- TounderstandhowEMIimpactswirelessandbroadbandtechnologies

UNITI INTRODUCTION&SOURCESOFEMINTERFERENCE 9

Introduction-Classificationofsources-Naturalsources-Man-madesources-Surveyofthe electromagnetic environment.

UNITII EMSHIELDING 9

Introduction-Shieldingeffectiveness-Far-fieldsources-Near-fieldsources-Low-frequency, magnetic field shielding - Effects of apertures

UNITIII INTERFERENCECONTROLTECHNIQUES 9

Equipmentscreening-Cablescreening-grounding-Power-linefilters-Isolation-Balancing- Signal-line filters - Nonlinear protective devices.

UNITIV EMCSTANDARDS,MEASUREMENTSANDTESTING 9

Needforstandards-TheinternationalframeworkHumanexposurelimitstoEMfields-EMC measurement techniques - Measurement tools - Test environments.

UNITV EMCCONSIDERATIONSINWIRELESSANDBROADBAND TECHNOLOGIES 9

Efficient use of frequency spectrum - EMC, interoperability and coexistence - Specifications and alliances - Transmission of high-frequency signals over telephone and power networks – EMC and digital subscriber lines - EMC and power line telecommunications.

SUGGESTEDACTIVITIES:

1. Investigatevarious casestudies relatedtoEMIC.Example:ChernobylDisasterin1986.
2. .DevelopsomeunderstandingaboutthedesignofEMshieldsinelectronicsystemdesign and packaging.

COURSEOUTCOMES:

Uponcompletionofthiscourse,thestudentwillbeableto

CO1: Demonstrate knowledge of the various sources of electromagnetic interference
CO2: Displayanunderstandingoftheeffectofhowelectromagneticfieldscouplethrough apertures, and solve simple problems based on that understanding
CO3: ExplaintheEMImitigationtechniquesofshieldingandgrounding
CO4: ExplainteneedforstandardsandEMCmeasurementmethods
CO5: DiscusstheimpactofEMConwirelessandbroadbandtechnologies

TOTAL:45PERIODS

REFERENCES

1. ChristopoulosC,PrinciplesandTechniquesofElectromagneticCompatibility,CRCPress, Second Edition, Indian Edition, 2013.

2. PaulCR,IntroductiontoElectromagneticCompatibility,WileyIndia,SecondEdition,2015.
3. KodaliVP,EngineeringElectromagneticCompatibility,WileyIndia,SecondEdition,2015
4. HenryWOtt,ElectromagneticCompatibilityEngineering,JohnWiley&SonsInc, Newyork,2016.
5. ScottBennett W, Control andMeasurement ofUnintentional Electromagnetic Radiation, John Wiley& Sons Inc., Wiley Interscience Series, 2015.

23VDP044 **DATACONVERTERS** **L TPC 3003**

COURSEOBJECTIVES:

- ToteachAnalogtoDigitalandDigitaltoAnalogConverterscharacteristics
- ToteachthedesignofSwitchedCapacitorbasedCircuits
- ToteachthedesignofAnalogtoDigitalandDigitaltoAnalogConverters

UNITI INTRODUCTION & CHARACTERISTICS OF AD/DA CONVERTERCHARACTERISTICS **9**

Evolution,TypesandApplicationsofAD/DAConverterCharacteristics,IssuesinSampling, Quantization and Reconstruction, Oversampling and Anti-aliasing Filters.

UNITII INTRODUCTIONTOTRACK-AND-HOLDAMPLIFIER **9**

Switched-CapacitorAmplifiers,SwitchedCapacitorIntegrator,SwitchedCapacitorCommonMode Feedback. Single Stage Amplifier as Comparator, Cascaded Amplifier Stages as Comparator, Latched Comparators. Offset Cancellation, Op Amp Offset Cancellation, Calibration Techniques

UNITIII NYQUISTRATED/ACONVERTERS **9**

CurrentSteeringDACs,CapacitiveDACs,BinaryWeightedVs.ThermometerDACS,Issuesin Current Element Matching, Clock Feed Through, Zero Order Hold Circuits.

UNITIV ADCARCHITECTURE **9**

PerformanceMetrics,FlashArchitecture,PipelinedArchitecture,SuccessiveApproximation Architecture,TimeInterleavedArchitecture,DNL,INLandOtherPerformanceMetricsofADCsand DACs.

UNITV SIGMADELTACONVERTERS **9**

STF,NTF,FirstOrderandSecondOrderSigmaDeltaModulatorCharacteristics,EstimatingThe MaximumStableAmplitude,CTDSMs,OpampNonlinearities

TOTAL:45PERIODS

COURSEOUTCOMES:

Attheendofthiscourse,thestudentswillbe

CO1:abletocarryoutthedesigncalculationsfordevelopingthevariousblocksassociatedwitha typical CMOS AD or DA Converter.

CO2:abletodesign andimplementcircuitsusingSwitchedCapacitorConcepts

CO3:abletoanalyzeanddesignD/AConverters

CO4:abletodesigndifferenttypesofA/Ds

CO5:abletoanalyzeanddesignSigmaDeltaconverter

REFERENCES

1. BehzadRazavi,"PrinciplesofDataConversionSystemDesign",IEEEPress,2015.
2. M.Pelgrom,"Analog-to-DigitalConversion",Springer,2015.
3. Rudy Van De Plassche, "CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters"KluwerAcedamicPublishers,Boston,2016.
4. J.G.Proakis,D.G.Manolakis,"DigitalSignalProcessingPrinciples,Algorithmsand Applications",PrenticeHall,4thEdition,2016.
5. ShanthiPavan,RichardSchreier,GaborC.Temes,"UnderstandingDelta-SigmaData Converters", Willey –IEEE Press, 2ndEdition,2017.

23VDP045	HARDWARESOFTWARECO-DESIGNFOR FPGA	L TPC 3003

COURSEOBJECTIVES:

- Toacquiretheknowledgeaboutsystem specificationandmodelling
- Tolearntheformulationofpartitioning
- Tostudythedifferenttechnicalaspects aboutprototypingandemulation

UNITI SYSTEMSPECIFICATIONANDMODELLING 9

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modeling, Co-Design for Heterogeneous Implementation - Processor Synthesis, Single-Core ArchitectureswithSingleASICandMultipleASICs,Multi-ProcessorArchitectures,ComparisonofCo-Design Approaches, Models of Computation, Requirements for Embedded System Specification

UNITII HARDWARE/SOFTWAREPARTITIONING 9

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of The Partitioning Graph, Formulation of The HW/SW Partitioning Problem, Optimization, HW/SW Partitioning Based On Heuristic Scheduling, HW/SW Partitioning Based On Genetic Algorithms.

UNITIII HARDWARE/SOFTWARECO-SYNTHESIS 9

TheCo-SynthesisProblem,State-TransitionGraph,RefinementandControllerGeneration, Distributed System Co-Synthesis

UNITIV PROTOTYPINGANDEMULATION 9

Introduction, Prototyping and Emulation Techniques, Prototyping and Emulation Environments, FutureDevelopmentsinEmulationandPrototyping,TargetArchitecture,ArchitectureSpecialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes,ArchitecturesforControl-DominatedSystems,ArchitecturesforData-DominatedSystems, Mixed Systems and Less Specialized Systems.

UNITV DESIGNSPECIFICATIONANDVERIFICATION 9

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design System-Level Specification, Design RepresentationforSystemLevelSynthesis,SystemLevelSpecificationLanguages, HeterogeneousSpecificationandMulti-LanguageCo-Simulation

TOTAL:45PERIODS

COURSEOUTCOMES:

Attheendofthiscourse,thestudentswillbeableto

CO1: DescribeTheBroadRangeofSystemArchitecturesandDesignMethodologiesthatcurrently exist and define their fundamental attributes.

CO2: DiscusstheDataflowModelsasaState-of-the-ArtMethodologytoSolveCo-Design Problems and to Optimize the balance between Software and Hardware.

CO3: UnderstandinTranslatingbetweenSoftwareandHardwareDescriptionsthroughCo-Design Methodologies.

CO4: UnderstandtheState-of-The-ArtpracticesindevelopingCo-DesignSolutionstoproblems using modern Hardware/Software Tools for building prototypes.

CO5: UnderstandtheConcurrentSpecificationfromanAlgorithm,Analyzeitsbehaviorand partitiontheSpecificationintoSoftware(CCode)andHardware(HDL)Components

REFERENCES

1. Patrick Schaumont, “A Practical Introduction to Hardware/Software Co-design”, Springer,2015
2. RalfNiemann,“Hardware/SoftwareCo-DesignforDataFlowDominatedEmbedded Systems”,Kluwer AcademicPublisher,2016.
3. JorgenStaunstrup,WayneWolf,“Hardware/SoftwareCo-Design:PrinciplesandPractice”, Kluwer Academic Publisher,2015
4. GiovanniDeMicheli,RolfErnstMorgon,“ReadinginHardware/SoftwareCo-Design”, Kaufmann Publisher,2021

23VDP046 POWERMANAGEMENTANDCLOCKDISTRIBUTIONCIRCUITS LTP C 3003

COURSEOBJECTIVES:

- todesignofreferencecircuitsandlowdropoutregulatorsfordesiredspecifications
- tounderstandoscillatorschoiceandrequirementsforclockgenerationcircuits
- todesignclockgenerationandrecoveryinthecontextofhighspeedsystems

UNITI VOLTAGEANDCURRENTREFERENCES 9

Currentmirrors,selfbiasedcurrentreference,startupcircuits,VBEbasedcurrentreference,VT basedcurrentreference,bandgapreference,temperatureindependentbiasing,constantGmbiasing.

UNITII LOWDROPOUTREGULATORS 9

Analogbuildingblocks,negativefeedback,performancemetrics,ACdesign,stability,internaland externalcompensation,PSRR-internalandexternalcompensationcircuits

UNITIII OSCILLATORFUNDAMENTALS 9

General considerations, ring oscillators, LC oscillators, Colpitts oscillator, jitter and phase noise in ring oscillators, impulse sensitivity function for LC & ring oscillators, phase noise in differential LC oscillators.

UNITIV CLOCKDISTRIBUTION CIRCUITS 9

PLLfundamental,PLLstability,noiseperformance,charge-pumpPLLtopology,CPPLLbuilding blocks, jitter and phase noise performance, DLL fundamentals.

UNITV CLOCKANDDATARECOVERYCIRCUITS 9

CDRarchitectures,transimpedance amplifiersandlimiters,CMOSinterface,linearhalfrateCMOS CDRcircuits,widecapturerangeCDRcircuits.

TOTAL:45PERIODS

COURSEOUTCOMES:

Attheendofthiscourse,thestudentswillbeableto:

CO1:designbandgapreferencecircuitsandlowdropoutregulatorforagivenspecification.

CO2:understand specificationrelatedtosupplyandclockgenerationcircuitsofIC

CO3: choose oscillator topology and design meeting the requirement of clock generation circuits.

CO4: design clockgenerationcircuitsin the contextofhigh speedI/Os, highspeed broad band communication circuits and data conversion circuits.

CO5:Designclockdistributioncircuits

REFERENCES

1. Gabriel.a.Rincon-Mora,"VoltageReferencesfromDiodetoPrecisionHigherOrderBand gapcircuits",JohnWiley&SonsInc,2015.
2. Gabriel.a.Rincon-Mora,"AnalogICDesignwithLow-DropoutRegulators",Mcgraw-Hill ProfessionalPub,2016.
3. BehzadRazavi,"DesignofAnalogCMOSIntegratedCircuits",TataMcgrawHill,2016
4. FloydM.Gardner,"PhaseLockTechniques"JohnWiley&Sons,Inc2015.

5.MichielSteyaert,ArthurH.M.VanRoermund,HermanCasier,“AnalogCircuitDesign:High SpeedClockandDataRecovery,High-PerformanceAmplifiersPowerManagement”, Springer, 2008.
6. Behzadrazavi,“DesignofIntegratedCircuits forOptical Communications”,McGraw Hill, 2015.

23VDP047	**RECONFIGURABLEARCHITECTURES**	**LTP C 3003**

COURSEOBJECTIVES:

- Thestudentshalldevelopanoverviewanddeeperinsightintotheresearchand development that is underway to meet future needs of flexible processors
- tolearntheconceptsofimplementation,synthesisandplacementofmodulesin reconfigurable architectures
- tounderstandthecommunicationtechniquesandSystemonProgrammableChipfor reconfigurable architectures
- tolearntheprocessofreconfigurationmanagement
- tofamiliarizetheapplicationsofreconfigurablearchitectures

UNIT– I INTRODUCTION 9

Generalpurposecomputing–domainspecificprocessors–ApplicationSpecificProcessors– reconfigurablecomputing–fieldsofapplication–evolutionofreconfigurablesystems–simple ProgrammableLogic Devices – Complex Programmable LogicDevices – Field Programmable Gate Arrays – coarse grained reconfigurable devices.

UNIT–II IMPLEMENTATION,SYNTHESISANDPLACEMENT 9

Integration – FPGA design flow – logic synthesis – LUT based technology mapping – modeling – temporalpartitioningalgorithms–offlineandonlinetemporalplacement–managingdevice'sfreeand occupied spaces.

UNIT–III COMMUNICATIONAND SOPC 9

Directcommunication– communicationoverthirdparty– busbasedcommunication– circuit switching–NetworkonChip–dynamicNetworkonChip–SystemonaProgrammableChip– adaptive multi-processing on chip.

UNIT–IV RECONFIGURATIONMANAGEMENT 9

Reconfiguration–configurationarchitectures–managingthereconfigurationprocess–reducing configuration transfer time – configuration security.

UNIT–V APPLICATIONS 9

FPGAbasedparallelpatternmatching -lowpowerFPGAbasedarchitectureformicrophonearrays in Wireless Sensor Networks - exploiting partial reconfiguration on a dynamic coarsegrained reconfigurable architecture – parallel pipelined OFDM baseband modulator with dynamic frequencyscalingfor5Gsystems.

TOTAL:45PERIODS

COURSEOUTCOMES:

Attheendofthiscourse,thestudentsshouldwillbeableto:

CO1:analyzethedifferentarchitectureprinciplesrelevanttoreconfigurablecomputing systems
CO2:comparethetradeoffsthatarenecessarytomeetthearea,powerandtimingcriteriaof reconfigurable systems
CO3:analyzethealgorithmsrelatedtoplacementandpartitioning
CO4:analyzethecommunicationtechniquesandsystemonprogrammablechipforreconfigurable architectures
CO5:analyzetheprinciplesofNetworkandSystemonaProgrammableChip

REFERENCES

1.ChristopheBobda,“IntroductiontoReconfigurableComputing:Architectures,Algorithms and Applications”, Springer 2015.

2.ScottHauckandAndreDehon,“ReconfigurableComputing:The Theory andPractice of FPGA Based Computation”, Elsevier 2016

3.M. Gokhale and P. Graham,“ReconfigurableComputing:AcceleratingComputationwith Field-Programmable Gate Arrays”, Springer, 2015.

4.NikoloasVorosEtAl.“AppliedReconfigurableComputing:Architectures,Toolsand Applications” Springer, 2018.

5.KoenBertels,JoãoM.P.Cardoso,StamatisVassiliadis,“ReconfigurableComputing: Architectures and Applications”, Springer 2016.

23VDP048 ADVANCED WIRELESSSENSORNETWORKS LTPC 3003

COURSEOBJECTIVES:

- to enable the student to understand the role of sensors and the networking of sensed data for different applications.
- to expose the students to the sensor node essentials and the architectural details, the medium access and routing issues and the energy constrained operational scenario.
- to enable the student to understand the challenges in synchronization and localization of sensor nodes, topology management for effective and sustained communication, data management and security aspects

UNITI OVERVIEWOFWIRELESS SENSORNETWORKS 9

Challengesforwirelesssensornetworks-characteristicsrequirements-requiredmechanisms, difference betweenmobile ad-hoc andsensor networks, applications ofsensor networks-case study, enabling technologies for wireless sensor networks, WLAN bands.

UNITII ARCHITECTURES 9

Single-node architecture - hardware components, energy consumption of sensor nodes , operating systemsandexecutionenvironments,networkarchitecture-sensornetworkscenarios,optimization goals andfiguresof merit,gatewayconcepts.Physical layerandtransceiverdesign considerations.

UNITIII MACANDROUTING 9

MAC protocols for wireless sensor networks, IEEE 802.15.4, Zigbee, low duty cycle protocols and wakeup concepts - s-MAC , the mediation device protocol, wakeup radio concepts, address and name management, assignment of MAC addresses, routing protocols- energy- efficient routing, geographic routing.

UNITIV INFRASTRUCTUREESTABLISHMENT 9

Topologycontrol,clustering,timesynchronization,localizationandpositioning,sensortaskingand control.

UNITV DATAMANAGEMENTANDSECURITY 9

Data management in WSN, storage and indexing in sensor networks, query processing in sensor, dataaggregation,directeddiffusion,tinyaggregation,greedyaggregation,securityinWSN,security protocols for sensor networks, secure charging and rewarding scheme, secure event and eventboundarydetection.

TOTAL:45 PERIODS

COURSEOUTCOMES:

Attheendofthiscourse,thestudentswillbeableto:

CO1:design and implement simple wireless network concepts

CO2:design,analyzeandimplementdifferentnetworkarchitectures

CO3:implement MAC layer and routing protocols

CO4:dealwithtimingandcontrolissuesinwirelesssensornetworks

CO5:analyzeanddesignsecuredwirelesssensornetworks

REFERENCES

1. HolgerKarl&AndreasWillig,"ProtocolsandArchitecturesforWirelessSensorNetworks", John Wiley, 2015.
2. ErdalÇayirci,ChunmingRong,“SecurityinWirelessAdHocand SensorNetworks”,John WileyandSons,2016.
3. KazemSohraby,DanielMinoli,&TaiebZnati,“WirelessSensorNetworks-STechnology, Protocols,andApplications”,JohnWiley,2016.
4. Yingshu Li, My T. Thai,Weili Wu, “Wireless Sensor Networks and Applications”, Springer, 2015.

23VDP049 SIGNALINTEGRITYFORHIGHSPEEDDESIGN LTPC
3 0 0 3

COURSEOBJECTIVES:

- Toidentifysourcesaffectingthespeedofdigitalcircuits.
- Tointroduce methodstoimprovethesignaltransmissioncharacteristics

UNITI SIGNALPROPAGATIONONTRANSMISSIONLINES 9

Transmission lineequations,wavesolution,wave*vs*.circuits,initial wave, delaytime, Characteristic impedance , wave propagation, reflection, and bounce diagrams Reactive terminations – L, C , static field maps of micro strip and strip line cross-sections, per unit length parameters,PCBlayerstackupsandlayer/Cuthicknesses,cross-sectionalanalysistools,ZoandTd equations for microstrip and stripline Reflection and terminations for logic gates, fan-out, logic switching , input impedance into a transmission-line section, reflection coefficient, skin-effect, dispersion.

UNITII MULTI-CONDUCTORTRANSMISSIONLINES ANDCROSS-TALK 9

Multi-conductor transmission-lines, coupling physics, per unit length parameters ,Near and far-end cross-talk, minimizing cross-talk (stripline and microstrip) Differential signalling, termination, balanced circuits ,S-parameters, Lossy and Lossless models.

UNITIII NON-IDEALEFFECTS 9

Non-ideal signal return paths – gaps, BGA fields, via transitions , Parasitic inductance and capacitance,Transmissionlinelosses–Rs,tanδ,routingparasitic,Common-modecurrent, differential-modecurrent,Connectors.

UNITIV POWERCONSIDERATIONSANDSYSTEMDESIGN 9

SSN/SSO , DC power bus design , layer stack up, SMT decoupling ,, Logic families, power consumption, and system power delivery , Logic families and speed Package types and parasitic ,SPICE, IBIS models ,Bit streams, PRBS and filtering functions of link-path components , Eye diagrams ,jitter , inter-symbol interference Bit-error rate ,Timing analysis.

UNITV CLOCKDISTRIBUTIONANDCLOCKOSCILLATORS 9

Timing margin, Clock slew, low impedance drivers, terminations, Delay Adjustments, canceling parasitic capacitance, Clock jitter.

TOTAL: 45PERIODS

COURSEOUTCOMES:

Attheendofthecoursethestudentwillbeableto

CO1: identify sources affecting the speed of digital circuits.

CO2:identifymethodstoimprovethesignaltransmissioncharacteristics

CO3: characterise and model multiconductor transmission line

CO4:analyseclockdistributionsystemandunderstanditsdesignparameters

CO5:analysenonidealeffectsoftransmission line

REFERENCES

1. H.W.JohnsonandM.Graham,High-SpeedDigitalDesign:AHandbookofBlackMagic, Prentice Hall, 2015.
2. DouglasBrooks,SignalIntegrityIssuesandPrintedCircuitBoardDesign,PrenticeHallPTR,2016.
3. S.Hall,G.Hall,andJ.McCall,High-SpeedDigitalSystemDesign:AHandbooofInterconnect Theory and Design Practices, Wiley-Interscience, 2015.
4. EricBogatin,SignalIntegrity-Simplified,PrenticeHallPTR,2015.

TOOLSREQUIRED

1. SPICE,source-http://www-cad.eecs.berkeley.edu/Software/software.html
2. HSPICEfromsynopsis,www.synopsys.com/products/mixedsignal/hspice/hspice.html
3. **SPECTRAQUEST**fromCadence,http://www.specctraquest.com **or any equivalent open source tool**

23VDP050 SYSTEMONCHIP LTPC
3003

COURSEOBJECTIVE:

- Tointroduce architectureanddesign conceptsunderlyingsystemonchips.
- StudentscangainknowledgeofdesigningSoCs.
- Toimpartknowledgeaboutthehardware-softwaredesignofamodestcomplexitychip allthe way from specifications, modeling, synthesis and physical design.

UNITI SYSTEMARCHITECTURE:OVERVIEW 9

Components of the system – Processor architectures – Memory and addressing – system levelinterconnection–SoCdesignrequirementsandspecifications–designintegration–design complexity – cycle time, die area and cost, ideal and practical scaling, area-time-power tradeoff in processordesign,Configurability.

UNITII PROCESSORSELECTIONFORSOC 9

Overview – soft processors, processor core selection. Basic concepts – instruction set, branches, interruptsandexceptions.Basicelementsininstructionhandling–Minimizingpipelinedelays– reducing the cost of branches – Robust processors – Vector processors, VLIW processors, Superscalar processors.

UNITIII MEMORYDESIGN 9

SoC external memory, SoC internal memory, Scratch pads and cache memory – cache organization and write policies – strategiesfor line replacement at miss time – split I- and Dcaches – multilevel caches – SoC memory systems – board based memory systems – simpleprocessor/memory interaction.

UNITIV INTERCONNECTARCHITECTURESANDSOCCUSTOMIZATION 9

Bus architectures – SoC standard buses – AMBA, CoreConnect– Processor customization approaches–Reconfigurabletechnologies –mappingdesignsontoreconfigurabledevices –FPGA based design – Architecture of FPGA, FPGA interconnect technology, FPGA memory, Floor plan and routing.

UNITV FPGABASEDEMBEDDEDPROCESSOR 9

Hardware software task partitioning – FPGA fabric Immersed Processors – Soft Processors andHardProcessors–ToolflowforHardware/SoftwareCo-design–InterfacingProcessorwith memoryandperipherals–Typesof On-chipinterfaces–Wishboneinterface,AvalonSwitchMatrix, OPB Bus Interface, Creating a Customized Microcontroller - FPGA-based Signal Interfacing and Conditioning.

TOTAL:45PERIODS

COURSEOUTCOMES:

Uponsuccessfulcompletionoftheprogramthestudentsshall

CO1: ExplainallimportantcomponentsofaSystem-on-Chipandanembeddedsystem,i.e.
CO2:digitalhardwareandembeddedsoftware;
CO3:Outlinethemajordesignflowsfordigitalhardwareandembeddedsoftware;
CO4: Discussthemajorarchitectures andtrade-offsconcerningperformance,costandpower
CO5:consumptionofsinglechipandembeddedsystems;

REFERENCES:

1. WayneWolf,“ModernVLSIDesign-System-on-ChipDesign”,PrenticeHall,3rdEdition, 2020.
2. WayneWolf,“ModernVLSIDesign-IPbasedDesign”,PrenticeHall,4thEdition,2018

23VDP051 **MEMSANDNEMS** **LTPC**
3003

COURSEOBJECTIVES:

- tointroducetheconceptsofMicroElectroMechanicaldevices.
- toknowthefabricationprocessof microsystems.
- toknowthedesignconceptsofmicrosensorsandmicroactuators.
- tofamiliarizeconceptsofQuantumMechanicsandNanosystems.

UNITI OVERVIEW **9**

New trends in Engineering and Science: Micro and Nanoscale systems, introduction to design of MEMS and NEMS, MEMS and NEMS – applications, devices and structures. Materials for MEMS: Silicon, Silicon compounds, polymers, metals

UNITII MEMSFABRICATIONTECHNOLOGIES **9**

Microsystem Fabrication Processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin FilmDepositions:LPCVD,Sputtering,Evaporation,Electroplating;EtchingTechniques:DryandWet Etching, Electrochemical Etching; Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect- Ratio (LIGA and LIGA-Like) Technology; Packaging: Microsystems Packaging, Essential Packaging Technologies, Selection of Packaging Materials

UNITIII MICRO SENSORS **9**

MEMS Sensors: Design of Acoustic Wave Sensors, Resonant Sensor, Vibratory Gyroscope, Capacitive and Piezo Resistive Pressure Sensors- Engineering Mechanics Behind These Microsensors. Case Study: Piezo-Resistive Pressure Sensor.

UNITIV MICROACTUATORS **9**

Design of Actuators: Actuation Using Thermal Forces, Actuation Using Shape Memory Alloys, Actuation Using Piezoelectric Crystals, Actuationusing Electrostatic Forces (ParallelPlate, Torsion Bar, Comb Drive Actuators), Micromechanical Motors and Pumps. Case Study: Comb Drive Actuators.

UNITV NANOSYSTEMSANDQUANTUMMECHANICS **9**

AtomicStructuresandQuantumMechanics,MolecularandNanostructureDynamics:Schrodinger EquationandWaveFunctionTheory,DensityFunctionalTheory,NanostructuresandMolecular Dynamics,ElectromagneticFieldsandtheirQuantization,MolecularWiresandMolecularCircuits

TOTAL:45 PERIODS

COURSEOUTCOMES:

Attheendofthiscourse,thestudentwillbeableto:

CO1: Discussmicrosensors

CO2: Explainmicro actuators

CO3: Outlinenanosystems andQuantummechanics

CO4: Designmicroactuatorsfordifferentapplications

CO5:Analyzeatomicstructures

REFERENCES

1. ChangLiu,“Foundations of MEMS”,PearsonEducationIndiaLimited,2016.
2. MarcMadou,“FundamentalsofMicrofabrication”,CRCPress2018.
3. StephenD.Senturia,”MicroSystemDesign”,Kluwer AcademicPublishers,2021
4. Sergey Edward Lyshevski, “MEMSandNEMS: Systems,Devices, and Structures”CRC Press, 2019.
5. TaiRanHsu,”MEMSandMicrosystemsDesignandManufacture”,TataMcrawHill,2022.

23VDP052 **NETWORKONCHIP** **LTPC**

3003

COURSEOBJECTIVES:

Thestudentsshouldbemadeto:

- UnderstandtheconceptofNetwork-on-Chip
- Learnrouterarchitecturedesigns
- StudyfaulttoleranceNetwork-on-Chip

UNITI INTRODUCTIONTOINTERCONNECTIONNETWORKS 9

Uses of Interconnection Networks, Network Basics, A Simple Interconnection Network, Network SpecificationsandConstraints,Topology,Routing,FlowControl,RouterDesign,PerformanceAnalysis.

UNITII TYPESOF NETWORKS 9

ButterflyNetworks,TorusNetworksMeshNetworks,Non-blockingnetworks,Non-interfacingnetworks, Crossbar networks Clos Networks, Bene˘s Networks, Sorting Networks

UNITIII ROUTING&FLOWCONTROL 9

Routing Basics, Deterministic Routing, Dimension-Order Routing, Adaptive Routing, Adaptive Routing Basics, Minimal Adaptive Routing, Fully Adaptive Routing, Flow control basics, Butterflow control, Buffer ManagementandBackpressure,Aflitreservationflowcontrol,Deadlockandlivelockavoidances,Deadlock and livelock avoidances in adaptive routing

UNITIV QUALITYOFSERVICE&ROUTER 9

Guranteedservices,Best-Effortservices,RouterDatapathComponents,InputBufferorganization, Switches, Output Organization, Arbitration, waveform allocator, Processor-Network Interface, Shared Memory Interface.

UNITV PERFORMANCEANALYSIS 9

Throughput,Latency,FaultTolerance,CommonMeasurementPitfallsQueuingTheory,Probabilistic Analysis, Application-Driven Workloads, Synthetic Workloads, Virtual Channels, Network Size, Injection Processes, Prioritization, Stability, Fault tolerance

TOTAL:45 PERIODS

COURSEOUTCOMES:

Attheendofthiscourse,thestudentswillbeableto:

CO1: Compare different architecture design

CO2: Discuss different routing algorithms

CO3: ExplainthreedimensionalNetworksonChiparchitectures

CO4:TestanddesignfaulttolerantNOC

CO5: DesignthreedimensionalarchitecturesofNOC

REFERENCES

1.ChrysostoMOSnicopoulos,VijaykrishnanNarayanan,ChitaR.Das"Networks-On-Chip "ArchitecturesHolistic Design Exploration", Springer.

2.Fayezgebali,Haythamelmiligi,HqhahedwatheqE1-Kharashi"Networks-On-ChipsTheory andPracticeCRC Press

3.KonstantinosTatasandKostasSiozios"Designing2Dand3DNetwork-On-Chip Architectures"2019

4. Palesi,Maurizio, Daneshtalab, Masoud"RoutingAlgorithmsinNetworks-On-Chip"2018

5. WilliamJamesDallyand BrianPatrickTowles,"PrinciplesandPracticesofInterconnection Networks",The Morgan Kaufmann Series in Computer Architecture and Design,2020.

23VDP053 **NANOTECHNOLOGY** **LTP C**
3003

COURSEOBJECTIVES:

- Providesknowledgeofvariousindustrialapplicationsof Nanotechnology
- Introducesthetheoryandpracticeon Nanomaterials
- Impartingthestateofartofnanotechnologytothesocietyandtotheenvironmental implication
- Toexercisethestudents'knowledgeandimaginationof Nanoscienceand nanotechnologytowardengineeringapplicationscoupledwithdetailedjustifications.

UNITI NANOTECHNOLOGY **9**

Background,whatis Nanotechnology,typesof NanotechnologyandNano-machines,topdownand bottomuptechniques,atomicmanipulation-Nanodots,semi-conductorquantumdots,self-assembly monolayers, simple details of characterization tools- SEM, TEM, STM, AFM.

UNITII NANOMATERIALS **9**

Whatare Nanomaterials,Preparationof Nanomaterials-solidstatereactionmethod,ChemicalVapor Deposition,SOL-GELStechniques,electrodeposition,ballmilling,introductiontolithography, Pulse Laser Deposition (PLD), applications of Nanomaterials, FinFET, TFET, QCA.

UNITIII CARBONTUBES **9**

Newformsofcarbon,carbontubes-typesof Nanotubes,formationof Nanotubes,assemblies, purification of carbon Nanotubes, properties of Nanotubes, applications of Nanotubes

UNITIV OPTICS,PHOTONICSANDSOLARENERGY **9**

LightandNanotechnology,interactionoflightandNanotechnology,Nanoholesandphotons,solar cells, optically useful Nanostructured polymers, photonic crystals.

UNITV FUTUREAPPLICATIONS **9**

MEMS, Nanomachines,Nanodevices, Quantum Computers, Opto-electronicDevices, Quantum Electronic devices, environmental and biological applications.

TOTAL:45 PERIODS

COURSEOUTCOMES:

Attheendofthiscourse,thestudentsshouldwillbeableto:

CO1:understandthebasesforintroductionto Nanotechnology

CO2:understandthesynthesisof Nanomaterialsandtheirapplicationandtheimpactof Nanomaterials on environment

CO3:acquireknowledgeaboutvariouskindof Nanomaterials

CO4:understand the Nanotechnologydevicesusedandtheirstructures

CO5:understandandimprovethe applicationof Nanotechnology

REFERENCES

1.Mick Wilson, Kamali Kannangra Geoff Smith, Michelle Simons and Burkhard Raguse,"Nanotechnology-BasicScienceandEmergingTechnologies",OverseasPress, 2015

2.MarkRatner andDaniel Ratner,"Nanotechnology-aGentleIntroduction toTheNextBig Idea",Prentice Hall,2016

3.RebeccaLJohnson,"Nanotechnology",LernerPublications,2015

4.CharlesP.PooleJr.,"IntroductiontoNanotechnogy",ChapmanandHall/CRS,2016

23VDP054 **EVOLVABLEHARDWARE** **LTPC**
3003

COURSEOBJECTIVES:

- Tostudyabouttheevolvablesystemsalgorithms,multi-objective utilityfunctions
- Understandtheconceptsofreliability,design-inredundancy,faulttoleranceand defect tolerance
- Design ofevolvable systems usingProgrammable Logic Devices (like FPGAs) and modularsubsystemswithidenticalcomponentsandgeneralizedcontrolleralgorithms

UNITI INTRODUCTION **9**

TraditionalHardwareSystemsanditsLimitations,EvolvableHardware,CharacteristicsofEvolvable Circuits and Systems, Technology-Extrinsic and Intrinsic Evolution offline and Online Evolution, Applications and Scope of EHW

UNITII EVOLUTIONARYCOMPUTATION **9**

Fundamentalsofevolutionaryalgorithms,componentsofEA,variantsofEA,GeneticAlgorithms, genetic programming, evolutionary strategies, evolutionary programming, implementations – evolutionarydesignandoptimizations,EHW-currentproblemsandpotentialsolutions

UNITIII RECONFIGURABLEDIGITALDEVICES **9**

Basicarchitectures-ProgrammableLogicDevices,FieldProgrammableGateArrays(FPGAS), usingreconfigurablehardware-designphase,executionphase,evolutionofdigitalcircuits

UNITIV RECONFIGURABLEANALOGDEVICES **9**

Basicarchitectures–FieldProgrammableTransistorArrays(FPTAS),analogarrays,MWMS, usingreconfigurablehardware-designphase,executionphase,evolutionofanalogcircuits

UNITV APPLICATIONSOFEHW **9**

Synthesisvs.Adaptation,designingself-adaptivesystems,fault-tolerantsystems,real-time systems,intrinsic reconfigurationforonline systems, EHW basedfault recoveryandfuture work

TOTAL:45 PERIODS

COURSEOUTCOMES:

Attheendofthiscourse,thestudentsshouldwillbeableto:

CO1: understandthefundamentals of computationalmodels andcomputers whichhaveappeared attheintersectionofhardwareandartificialintelligencetosolvehardcomputationalproblems.

CO2:understandthe principles ofbio-inspiredandunconventionalcomputationalsystems.

CO3:discussaboutthereconfigurabledigitalarchitecturesanditscomputationalintelligence techniques.

CO4:discussaboutthereconfigurableanalogarchitecturesanditscomputationalintelligence techniques.

CO5:discussaboutthetypicalapplicationsofbio-inspiredandotherunconventionaltechniquesin the phase of design, implementation and runtime of a computational device.

REFERENCES

1.GarrisonW.GreenwoodandAndrewM.Tyhrrell,"IntroductiontoEvolvableHardware:a PracticalGuideforDesigningSelf-AdaptiveSystems",Wiley-IeeePress,2016.

2.TetsuyaHiguchi,XinYaoandYongLiu,"EvolvableHardware",Springer-Verlag,2020.

3.LukasSekanina,"EvolvableComponents:FromTheorytoHardwareImplementations", Springer, 2020

23VDP055 **QUANTUM COMPUTING** **LTPC**

3003

OBJECTIVES:

- Toknowthebackgroundofclassicalcomputingandquantumcomputing.
- Tolearnthefundamentalconceptsbehindquantumcomputation.
- TostudythedetailsofquantummechanicsandtherelationtoComputerScience.
- Togainknowledgeaboutthebasichardwareandmathematicalmodelsof quantum computation.
- Tolearnthebasicsofquantuminformationandthetheorybehind it.

UNITI FUNDAMENTALCONCEPTS **9**

Global Perspectives – Quantum Bits – Quantum Computation – Quantum Algorithms-ExperimentalQuantumInformationProcessing-QuantumInformation.

UNITII QUANTUMMECHANICSANDOVERVIEWOFCOMPUTATIONALMODELS9

QuantumMechanics:LinearAlgebra-PostulatesofQuantumMechanics-Application: Superdense Coding – Density Operator – The Shmidt Decomposition and Purifications – EPR and the BellInequality – Computational Models: Turing Machines – Circuits-AnalysisofComputationalProblems.

UNITIII QUANTUMCOMPUTATION **9**

QuantumCircuits:QuantumAlgorithms-UniversalQuantumGates -Quantum CircuitModelofComputation–Simulation–QuantumFourierTransformand Applications- QuantumSearchAlgorithms- QuantumComputers

UNITIV QUANTUM INFORMATION **9**

QuantumNoiseandQuantumOperations: Classical Noiseand Markovprocesses — Quantum Operations — Examples— Applications— Distance Measures for QuantumInformation- Quantum ErrorCorrection- Entropy

UNITV QUANTUMINFORMATIONTHEORY **9**

Quantum States and Accessible Information – Data Compression – Classical Information Over Noisy Quantum Channels – Quantum Information Over Noisy Quantum Channels – Entanglement as a Physical Resource – Quantum Cryptography.

TOTAL:45PERIODS

OUTCOMES:

Oncompletionofthecourse,thestudentwillbeableto:

1. Understandthebasicsofquantumcomputing.
2. UnderstandthebackgroundofQuantumMechanics.
3. Analysethecomputation models.
4. Modelthecircuitsusingquantumcomputation.
5. Understandthequantumoperationssuchasnoiseanderror-correction.
6. Appreciatetheneedofquantumcomputing.

TEXTBOOKS:

1. MichaelA.Nielsen,IssacL.Chuang,“QuantumComputationand QuantumInformation”,TenthEdition,CambridgeUniversityPress,2015.

REFERENCES:

1. ScottAaronson,“QuantumComputingSinceDemocritus”,Cambridge University Press, 2016.
2. N. David Mermin, “Quantum Computer Science: An Introduction”, Cambridge University Press, 2015.

23VDP056 SOFTCOMPUTINGANDOPTIMIZATIONTECHNIQUES LTPC
3024

COURSEOBJECTIVE:

- Toclassifyvarioussoftcomputingframeworks.
- Tobefamiliarwiththedesignofneuralnetworks,fuzzylogic,andfuzzysystems.
- Tolearnmathematicalbackgroundforoptimizedgeneticprogramming.
- Beexposedtoneuro-fuzzyhybridsystemsanditsapplications.
- Tounderstandthevariousevolutionaryoptimization techniques.

UNITI FUZZYLOGIC: 9

IntroductiontoFuzzylogic-FuzzysetsandmembershipfunctionsOperationsonFuzzysets-Fuzzy relations, rules, propositions, implications, and inferences- Defuzzification techniques- Fuzzy logic controller design- Some applications of Fuzzy logic.

UNITII ARTIFICIALNEURALNETWORKS: 9

SupervisedLearning:Introductionandhowbrainworks,Neuronasasimplecomputingelement,The perceptron, Backpropagation networks: architecture, multilayer perceptron, backpropagation learning-input layer, accelerated learning in multilayer perceptron, The Hopfield network, Bidirectional associative memories (BAM), RBF Neural Network.

Unsupervised Learning: Hebbian Learning, Generalized Hebbian learning algorithm, Competitive learning, Self- Organizing Computational Maps: Kohonen Network.

UNITIII GENETICALGORITHM: 9

Geneticalgorithm-Introduction-biologicalbackground-traditionaloptimizationandsearch techniques - Geneticbasicconcepts - operators– Encodingscheme– Fitness evaluation – crossover-mutation-TravellingSalesmanProblem,Particleswamoptimization,Antcolony optimization.

UNITIV NEURO-FUZZYMODELING 9

Adaptive Neuro-Fuzzy Inference Systems(ANFIS) – architecture- Coactive Neuro-Fuzzy Modeling, framework, neuron functions for adaptive networks – Data Clustering Algorithms – Rule base Structure Identification –Neuro-Fuzzy Control – the inverted pendulum system.

UNITV CONVENTIONALOPTIMIZATIONTECHNIQUES 9

Introduction to optimization techniques, Statement of an optimization problem, classification, Unconstrained optimization-gradient search method-Gradient of a function, steepest gradient-conjugate gradient, Newton's Method, Marquardt Method, Constrained optimization –sequential linear programming, Interior penalty function method, external penalty function method.

TOTAL:45PERIODS

PRACTICAL EXERCISES:

Simulations using Python/MATLAB or Equivalent Open-Source Tools

1. Design and Implementation of a Fuzzy Logic Controller
2. Implementation of Artificial Neural Network Models for Classification
3. Implementation of Genetic Algorithm for Optimization Problems
4. Design and Implementation of an Adaptive Neuro-Fuzzy Inference System (ANFIS)
5. Implementation of Evolutionary Optimization Techniques (Particle Swarm Optimization/Ant Colony

Optimization)

COURSEOUTCOMES:

UponCompletionofthecourse,thestudentswillbeableto:

CO1: DevelopapplicationondifferentsoftcomputingtechniqueslikeFuzzy,GAandNeural network

CO2: ImplementNeuro-FuzzyandNeuro-Fuzz-GAexpertsystem.

CO3: Implementmachinelearningthrough Neuralnetworks.

CO4: ModelNeuroFuzzysystemforclusteringandclassification.

CO5: Abletousetheoptimizationtechniquestosolvetherealworldproblems

REFERENCES:

1. J.S.R.Jang,C.T.SunandE.Mizutani,Neuro-FuzzyandSoftComputing,PHI/PearsonEducation 2004.
2. DavidE.Goldberg,GeneticAlgorithmsinSearch,OptimizationandMachineLearning,Addison wesley, 2009.
3. GeorgeJ.KlirandBoYuan,FuzzySetsandFuzzyLogic-Theoryand Applications,Prentice Hall, 1995.
4. JamesA.FreemanandDavidM.Skapura,NeuralNetworksAlgorithms,Applications,and Programming Techniques, Pearson Edn., 2003.
5. Jyh-ShingRogerJang,Chuen-Tsai Sun,EijiMizutani,Neuro-FuzzyandSoftComputing, Prentice-Hall of India, 2003.
6. MitchellMelanie,AnIntroductiontoGeneticAlgorithm,PrenticeHall,1998.
7. SimonHaykins,NeuralNetworks:A ComprehensiveFoundation,PrenticeHallInternational Inc, 1999.
8. TimothyJ.Ross,FuzzyLogicwithEngineeringApplications,McGraw-Hill,1997.

23VDP057 VLSIFORWIRELESSCOMMUNICATION L TPC 3024

COURSEOBJECTIVES:

- Tounderstand theconceptsofbasicwirelesscommunicationconcepts.
- Tostudytheparametersinreceiverandlownoiseamplifierdesign.
- Tostudythevarioustypesofmixersdesignedforwirelesscommunication.
- TostudyanddesignPLLand VCO.
- To understand the concepts of transmitters and power amplifiers in wireless communication.

UNITI COMMUNICATIONCONCEPTS 9

Introduction-Overview of Wirelesssystems-Standards- AccessMethods -Modulation schemes – Classicalchannel– Wirelesschanneldescription– Pathloss– Multipathfading– Standard Translation.

UNITII RECEIVERARCHITECTURE&LOWNOISEAMPLIFIERS 9

Receiverfrontend–Filterdesign–Non-idealities–Designparameters–Noisefigure&Input intercept point. LNA Introduction - Wideband LNA design - Narrow band LNA design: Impedance matching & Core amplifier.

UNITIII MIXERS 9

BalancingMixer-QualitativeDescriptionof theGilbertMixer-ConversionGain-Distortion-Noise - A Complete Active Mixer. Switching Mixer – Distortion, Conversion Gain & Noise in Unbalanced Switching Mixer - A Practical Unbalanced Switching Mixer. Sampling Mixer - Conversion Gain, Distortion, Intrinsic & Extrinsic Noise in Single Ended Sampling Mixer.

UNITIV FREQUENCYSYNTHESIZERS 9

PLL–Phasedetector–Dividers-VoltageControlledOscillators-LCoscillators–RingOscillators – Phasenoise–Loopfilters&designapproaches-Acompletesynthesizerdesignexample(DECT) – Frequency synthesizerwithfractionaldivider.

UNITV TRANSMITTERARCHITECTURES&POWERAMPLIFIERS 9

Transmitterbackenddesign–Quadrature LOgenerator–Poweramplifierdesign.

COURSEOUTCOMES:

Attheendofthiscourse,thestudentshouldbeableto

CO1: Abletorecollectbasicwirelesscommunicationconcepts.

CO2: Tounderstandtheparametersinreceiveranddesignalownoiseamplifier

CO3: Inapositiontoapplyhisknowledgeonvarioustypesofmixersdesignedforwireless communication.

CO4: DesignPLLandVCO

CO5: Understandtheconceptsoftransmittersandutilizethepoweramplifiersinwireless communication.

TOTAL:45PERIODS

PRACTICAL EXERCISES

Simulations using MATLAB/ EDA/SPICE/Equivalent Open-Source tools

1. Design and Simulation of a CMOS Low Noise Amplifier (LNA)
2. Design and Simulation of a CMOS Gilbert Cell Mixer
3. Design and Simulation of a CMOS Ring Voltage-Controlled Oscillator (VCO)
4. Design and Simulation of a CMOS Phase-Locked Loop (PLL) Frequency Synthesizer
5. Design and Simulation of a CMOS RF Power Amplifier (PA)

23VDP058 **PATTERNRECOGNITION** **LTPC**
3024

COURSEOBJECTIVES:

- Understandthein-depthconceptofPatternRecognition
- ImplementBayesDecisionTheory
- Understandthein-depthconceptofPerceptionandrelatedConcepts
- UnderstandtheconceptofMLPatternClassification
- UnderstandtheconceptofDLPatternRecognition

UNITI PATTERNRECOGNITION **8**

Induction Algorithms. Rule Induction. Decision Trees. BayesianMethods. Overview.NaiveBayes. The Basic Na¨ıve Bayes Classifier. Naive Bayes Induction for Numeric Attributes. Correction to the Probability Estimation. Laplace Correction. No Match. Other Bayesian Methods. Other Induction Methods.NeuralNetworks.GeneticAlgorithms.Instance-basedLearning.SupportVectorMachines.

UNITII STATISTICALPATTERNRECOGNITION **8**

AboutStatisticalPatternRecognition.Classificationandregression.Features,FeatureVectors,and Classifiers. Pre-processing and feature extraction. The curse of dimensionality. Polynomial curve fitting. Model complexity. Multivariate non-linear functions. Bayes' theorem. Decision boundaries. Parametricmethods.Sequentialparameterestimation.Linear discriminantfunctions. Fisher'slinear discriminant. Feed-forward network mappings.

UNITIII BAYESDECISIONTHEORYCLASSIFIERS **11**

Bayes Decision Theory. Discriminant Functions and Decision Surfaces. The Gaussian Probability Density Function. The Bayesian Classifier for Normally Distributed Classes. Exact interpolation. Radial basis function networks. Network training. Regularization theory. Noisy interpolation theory. Relationtokernelregression.Radialbasisfunctionnetworksforclassification.Comparisonwiththe multi-layerperceptron.Basisfunctionoptimization.

UNITIV LINEARDISCRIMINANTFUNCTIONS **9**

Linear Discriminant Functions and Decision Surfaces. The Two-Category Case. The Multicategory Case. The Perceptron Criterion Function. Batch Perceptron. Perceptron Algorithm Convergence. The Pocket Algorithm. Mean Square Error Estimation. Stochastic Approximation and the LMS Algorithm.ConvergenceProofforSingle-SampleCorrection.Fixedincrementdescent.SomeDirect Generalizations. Fixed increment descent. Batchvariable increment Perceptron. BalancedWinnow algorithm.RelaxationProcedures.TheDescentAlgorithm

UNITV NONLINEARCLASSIFIERS 9

The Two Layer Perception. The Three Layer Perception. Algorithms Based On Exact Classification OfThe Training Set. Feedforward operation and classification. General feedforward operation. Expressive power of multilayer networks. Backpropagation algorithm. Network learning. Training protocols. Stochastic Backpropagation. Batch Backpropagation. Radial basis function networks (RBF).Specialbases.Timedelayneuralnetworks(TDNN).Recurrentnetworks.Counter propagation.Cascade-Correlation.Cascade-correlation.Neocognitron

TOTAL: 45PERIODS

SUGGESTEDACTIVITIES:

1:CarSalesPatternClassificationusingSupportVectorClassifier 2:
Avocado Sales Pattern Recognition using Linear regression
3:TrackingMovementsbyimplementingPatternRecognition
4: Detecting Lanes by implementing Pattern Recognition
5:PatternDetectioninSARImages

COURSEOUTCOMES:

CO1: Discoverimaging,andinterpretationoftemporalpatterns
CO2: IdentifyStructuralData Patterns
CO3: ImplementPatternClassificationusingMachineLearning Classifiers
CO4: ImplementPatternRecognitionusingDeepLearningModels
CO5: ImplementImagePatternRecognition

PRACTICAL EXERCISES:

Simulations using Python/MATLAB or Equivalent Open-Source Tools

1. Implementation of Decision Tree and Naïve Bayes Classifiers for Pattern Recognition
2. Implementation of Feature Extraction and Statistical Pattern Classification
3. Implementation of Bayes Decision Theory and Gaussian Classifier
4. Implementation of Linear Discriminant Analysis (LDA) and Perceptron Classifier
5. Implementation of Deep Neural Network-Based Pattern Recognition

REFERENCES

I.PatternClassification,2ndEdition,RichardO.Duda,PeterE.Hart,andDavidG.Stork. Wiley, 2015

2.PatternRecognition,JürgenBeyerer,MatthiasRichter,andMatthiasNagel. 2018

3.PatternRecognitionandMachineLearning,ChristopherM.Bishop.Springer,2016

4.PatternRecognitionandClassification,Dougherty,andGeoff.Springer,2017

5.PracticalMachineLearningandImageProcessing,HimanshuSingh.Apress,2019

23VDP059	SYSTEMVERILOG	LTPC 3024

COURSEOBJECTIVES:

- InsighttoApplySystemVerilogConceptstoDoSynthesis,AnalysisandArchitectureDesign.
- UnderstandingofSystemVerilogandSVAforVerificationandUnderstandTheImprovements in Verification Efficiency.
- UnderstandAdvancedVerificationFeatures,SuchAsThePracticalUseofClasses, Randomization, Checking, and Coverage.
- KnowledgetoCommunicateThePurposeandResultsofaDesignExperimentinWrittenand Oral
- UnderstandThePurposeofHardware-SoftwareVerification

UNIT I VERIFICATIONMETHODOLOGY **9**

Verification Guidelines: Introduction, Verification Process, Verification Plan, Verification Methodology Manual, BasicTestbench Functionality, DirectedTesting, Methodology Basics, Constrained-Random Stimulus, Functional Coverage, Testbench Components, Layered Testbench

UNITII SYSTEMVERILOGBASICSANDCONCEPTS **9**

DataTypes:Built-inDataTypes,Fixed-SizeArrays,DynamicArrays,Queues,CreatingNewTypes WithTypedef,CreatingUser-DefinedStructures,EnumeratedTypes,Constants,Strings.Procedural Statements and Routines: Procedural Statements, Tasks, Functions, and Void Functions

UNITIII OOPS **9**

Introduction-Where to Define a Class- OOPS Terminology -Creating New Objects -Object Deallocation-UsingObjects-StaticVariablesVs.GlobalVariables-ClassRoutines-DefiningRoutines Outside of The Class - Scoping Rules -Using One Class Inside Another -Understanding Dynamic Objects -Copying Objects -Public Vs. Private -Straying Off Course - Building a Testbench

UNITIV THREADSANDINTER-PROCESS COMMUNICATIONAND FUNCTIONAL COVERAGE **9**

Working With Threads, Inter-Process Communication, Events, Semaphores, Mailboxes, Building a Testbench With Threads and IPC. Coverage Types, Functional Coverage Strategies, Simple FunctionalCoverageExample,CoverageOptions,ParameterizedCoverGroups,AnalysingCoverage Data, Measuring Coverage Statistics

UNITV COMPLETEDESIGNMODELUSINGSYSTEMVERILOG-CASESTUDY **9**

SystemVerilogATMExample,DataAbstraction,InterfaceEncapsulation,DesignTopLevelSquat, Receivers and Transmitters, Test Bench for ATM.

TOTAL:45 PERIODS

PRACTICALEXERCISES: **15PERIODS**

1. DesignaTestbenchfor2x1MuxUsingGates
2. ImplementationofaMailboxByAllocatingMemory
3. ImplementationandTestingofSemaphoreforaSimpleDUT
4. ImplementationofScoreboardforaSimpleDUT

TOTAL:45+15= 60PERIODS

COURSEOUTCOMES:

Uponcompletionofthiscourse,studentsshoulddemonstratetheabilityto

CO1:usesystem63erilogtocreatecorrect,efficient,andre-usablemodelsfordigitaldesigns

CO2:usesystem63erilogtocreatetestbenchesfordigitaldesigns

CO3:understandandeffectivelyexploitnewconstructsinSystemVerilogforverification

CO4:understandthecommunicationbetween modules

CO5:designingacompletesystemmodelusingVerilog

REFERENCES

1. SystemVerilogforVerification:aGuidetoLearningTheTestbenchLanguageFeatures,Chris Spear,Springer2015

2.WritingTestbenches:FunctionalVerificationofHDLModels,SecondEdition,JanickBergeron, KluwerAcademic Publishers,2016.

3.SystemVerilogforDesign:aGuidetoUsingSystemVerilogforHardwareDesignandModeling, 2nd Edition,StuartSutherland,SimonDavidmanandPeterFlake,Springer

4.OpenVerificationMethodologyCookbook,MarkGlasser,Springer,2016

5.Assertion-BasedDesign,2nd Edition,HarryD.Foster,AdamC.Krolnik,DavidJ.Lacey,Kluwer Academic Publishers, 2015

23VDP060 **MACHINE LEARNING** **L TPC**
3024

COURSEOBJECTIVES:

- Tounderstandtheconceptsandmathematicalfoundationsofmachinelearningandtypesof problems tackled by machine learning
- Toexplorethedifferentsupervisedlearningtechniquesincluding ensemblemethods
- Tolearndifferentaspectsofunsupervised learningandreinforcementlearning
- Tolearntheroleofprobabilisticmethodsformachinelearning
- Tounderstandthebasicconceptsofneuralnetworksanddeeplearning

UNITI INTRODUCTIONANDMATHEMATICALFOUNDATIONS 9

MachineLearning Basics -Need–History–Definitions–Applications–Advantages,Disadvantages & Challenges –Types of Machine Learning Problems – Mathematical Foundations – Linear Algebra & Analytical Geometry –Probability and Statistics- Bayesian Conditional Probability-Vector Calculus & Optimization – Decision Theory – Information theory

UNITII SUPERVISEDLEARNING 9

Introduction-DiscriminativeandGenerativeModels-LinearRegression-LeastSquares-Under-fitting /Overfitting-Cross-Validation-LassoRegression-Classification-LogisticRegression-GradientLinear Models –Support Vector Machines –Kernel Methods –Instance based Methods – K-Nearest Neighbours-Tree based Methods –Decision Trees –ID3 – CART – Ensemble Methods –Random Forest – EvaluationofClassificationAlgorithms

UNITIII UNSUPERVISEDLEARNINGANDREINFORCEMENTLEARNING 9

Introduction – Clustering Algorithms –K – Means – Hierarchical Clustering – Cluster Validity – Dimensionality Reduction –Principal Component Analysis – Recommendation Systems - EMalgorithm. Reinforcement Learning – Elements –Model based Learning – Temporal Difference Learning

UNITIV PROBABILISTICMETHODSFORLEARNING- 9

Introduction–NaïveBayesAlgorithm–MaximumLikelihood–MaximumApriori–BayesianBelief Networks –Probabilistic Modelling of Problems –Inference in Bayesian Belief Networks – Probability Density Estimation– Sequence Models – Markov Models – Hidden Markov Models

UNITV NEURALNETWORKSANDDEEPLEARNING 9

NeuralNetworks- BiologicalMotivation- Perceptron- Multi-layer Perceptron- FeedForwardNetwork-BackPropagation-ActivationandLossFunctions-LimitationsofMachineLearning-DeepLearning-ConvolutionNeuralNetworks-RecurrentNeuralNetworks-Usecases

45PERIODS

SUGGESTEDACTIVITIES:

1. Giveanexamplefromourdailylifeforeachtypeofmachinelearningproblem
2. Studyatleast3ToolsavailableforMachineLearninganddiscusspros&consofeach
3. Takeanexampleofaclassificationproblem.Drawdifferentdecisiontreesfortheexample and explain the pros and cons of each decision variable at each level of the tree
4. Outline10machinelearningapplicationsinhealthcare
5. Give5exampleswheresequentialmodelsaresuitable.
6. Giveatleast5recentapplicationsofCNN

PRACTICALEXERCISES: **15 PERIODS**

1. Implement a Linear Regression with a Real Dataset (https://www.kaggle.com/harrywang/housing).Experimentwithdifferentfeaturesinbuilding amodel.Tunethemodel'shyperparameters.
2. Implementabinaryclassificationmodel.Thatis,answersabinaryquestionsuchas"Arehouses in this neighborhood above a certain price?"(use data from exercise 1). Modify the classification threshold and determine how that modification influences the model. Experiment with different classification metrics to determine your model's effectiveness.
3. Classification with Nearest Neighbours. In this question, you will use the scikit-learn's KNN classifertoclassifyrealvs.fakenewsheadlines.Theaimofthisquestionisforyoutoreadthe

4. TomMMitchell,"MachineLearning",McGrawHillEducation,2013.
5. PeterFlach,"MachineLearning:TheArtandScienceofAlgorithmsthatMakeSenseofData", First Edition, Cambridge University Press, 2012.
6. ShaiShalev-ShwartzandShaiBen-David,"UnderstandingMachineLearning:FromTheorytoAlgorithms", Cambridge University Press, 2015
7. ChristopherBishop,"PatternRecognitionandMachineLearning",Springer,2007.
8. HalDauméIII,"ACourseinMachineLearning",2017(freelyavailableonline)
9. TrevorHastie,RobertTibshirani,JeromeFriedman,"The Elements ofStatistical Learning", Springer, 2009 (freely available online)
10. AurélienGéron,Hands-OnMachineLearningwithScikit-LearnandTensorFlow:Concepts, Tools, and Techniques to Build Intelligent Systems 2nd Edition, o'reilly, (2017)

Total: 60 Periods

23VDP061 ADAPTIVESIGNALPROCESSING LTPC 3024

COURSEOBJECTIVES:

- tounderstandthebasicprinciplesofdiscreterandomsignalprocessing
- tounderstandtheprinciplesofspectralestimation
- tolearnabouttheweinerandadaptivefilters
- tounderstand thedifferentsignal detectionand estimationmethods
- toacquireskillstodesignsynchronizationmethodsforproperfunctioningofthesystem

UNITI DISCRETERANDOMSIGNALPROCESSING 9

DiscreteRandomProcesses,RandomVariables,Parseval'sTheorem,Wiener-KhintchineRelation, Power Spectral Density, Spectral Factorization, Filtering Random Processes, Special Types of Random Processes

UNITII SPECTRALESTIMATION 9

Introduction, Nonparametric Methods – Periodogram, Modified Periodogram, Bartlett, Welch and Blackman-TukeyMethods,ParametricMethods–ARMA,ARandMAModelBasedSpectral Estimation, Solution Using Levinson-Durbin Algorithm.

UNITIII WEINERANDADAPTIVEFILTERS 9

WeinerFilter:FIRWienerFilter,IIRWienerFilter,AdaptiveFilter:FIRAdaptiveFilters-Steepest Descent Method- LMS Algorithm, RLS Adaptive Algorithm, Applications.

UNITIV DETECTIONANDESTIMATION 9

BayesDetectionTechniques,Map,Ml,-DetectionofM-ArySignals,Neymanpearson,Minimax Decision Criteria. Kalman Filter- Discrete Kalman Filter, The Extended Kalman Filter, Application.

UNITV SYNCHRONIZATION 9

SignalParameterEstimation,CarrierPhaseEstimation,SymbolTimingEstimator,JointEstimation ofCarrierPhaseandSymbolTiming.

TOTAL:45PERIODS

PRACTICALEXERCISE 15PERIODS

1. DesignofNon-ParametricandParametricforSpectralEstimation
2. DesignofLinearPredictionFilterUsingMatlab
3. DesignofLMSFilterUsingMatlab
4. DesignofRLSFilterUsingMatlab
5. DesignofExtendedKalmanFilterUsingMatlab

COURSEOUTCOMES: TOTAL : 60 PERIODS

On successful completion of this course, students will be able to

CO1: Analyzethebasicprinciplesofdiscreterandomsignalprocessing

CO2:Analyze the principles of spectral estimation

CO3:AnalyzetheWeinerandAdaptivefilters

CO4:Analyzethedifferentsignaldetectionandestimationmethods

CO5:Designthesynchronizationmethodsforproperfunctioningofthesystem

REFERENCES

1. Monson H. Hayes, "Statistical Digital Signal Processing and Modeling", JohnWileyand Sons, Inc, Singapore, 2015.
2. JohnG.Proakis.,"DigitalCommunication",4th Edition,McGrawHillPublications,2016.
3. SimonHaykin,"AdaptiveFilterTheory",PearsonEducation,FourthEdition,2015
4. BernardSklarandPabitraKumarRoy,"DigitalCommunications:Fundamentalsand Applications", 2/E, Pearson Education India, 2015
5. PauloS.R.Diniz,"AdaptiveFilteringAlgorithmsandPracticalImplementation",Springer,2016

23VDP062 VLSIARCHITECTURESFORIMAGEPROCESSING L TPC 3024

COURSEOBJECTIVES:

- Thestudentswillbeabletoacquireknowledgeonimageandvideoprocessingalgorithms
- Thestudentswillbeabletoacquireknowledgeondesignof VLSIarchitectures.

UNITI IMAGEPROCESSINGALGORITHMSANDARCHITECTURES 9

ImageProcessingTasks -LowLevelImageProcessingOperations -IntermediateLevelOperations Image Processor Architecture: Requirements and Classification - Uniand Multi Processors - MIMD Systems - SIMD Systems - Pipelines - Design Aspects of Real Time Low Level ImageProcessors-DesignMethodforSpecialArchitectures

UNITII 3DIMAGEPROCESSING 9

Overviewof3DImage -TypesandCharacteristicsof3DImageProcessing -Examplesof3DImage Processing, Continuous and Digitized Images, Models of Image Operations, Algorithm of Image Operations-Smoothing Filter-DifferenceFilter-DifferentialFeaturesof aCurvedSurface-Region Growing.

UNITIII 3DBINARYIMAGEPROCESSING 9

Introduction- Labeling of a Connected - Shrinking- Surface Thinning and Axis Thinning-Distance Transformation and Skeleton-Border Surface Following-Knot and Link .- Voronoi Division of a Digitized Image-Algorithms for Processing Connected Components with Gray Values

UNITIV PIPELINED,2DAND3DIMAGEPROCESSINGARCHITECTURES 9

Architecture of a Cellular Logic Processing Element - Second Decomposition in Data Path and Control-RealTimePipelineforLowLevelImageProcessing -DesignAspectsofImageProcessing Architectures - Implementation of Low Level 2D and 3D and Intermediate Level Algorithms

UNITV VLSISYSTEMSFORIMAGEPROCESSING 9

Concurrent Systems for Image Analysis- VLSI Wavefront Arrays for Image Processing-Curve Detection in VLSI-Design of VLSI Based Multicomputer Architecture for Dynamic Scene Analysis-VLSI-Based Image Resampling for Electronic Publishing

TOTAL:45PERIODS

PRACTICALEXERCISES:

1. Converta2DImageto3DImage.
2. ObtainaCTScanImage,PerformTheFollowing
   a. SmoothFilter
   b. DetectionFilter
   c. MorphologicalFilter
   d. RegionGrowing
3. PerformSurfaceThinningandAxisThinning,DistanceTransformationandSkeleton,Voronoi Division of a Digitized Image

TOTAL:45+15= 60PERIODS

COURSEOUTCOMES:

Upon Completion of The Course, StudentsWill Be Able to Demonstrate An Ability to
CO1: AnalyzeVariousArchitecturestoRealizeImageProcessingAlgorithmsandExplainThe3D Image Processing Algorithms
CO2: ExploreVariousProcessingTechniquesofImageandDesignDifferentArchitecturesfor ImageProcessing.
CO3: Analyzevariouspipelinedhardwarearchitecturefor2Dand3DImageprocessing
CO4: RealizebinaryimageprocessingalgorithminVLSIsystems
CO5: Implementfiltertechniquesin2Dand3Dimage.

REFERENCES

1. PieterJonker,"MorphologicalImageProcessing:ArchitectureandVLSIDesign",Springer, First Edition,2018.

2.JunichiroToriwaki·HiroyukiYoshida,"FundamentalsofThree-DimensionalDigitalImage Processing",Springer2019.

3.King-SunFu,"VLSIforPatternRecognitionandImageProcessing",Springer-Verlag,2015.

23VDP063 **DSPSTRUCTURESFORVLSI** **LTPC 3024**

COURSEOBJECTIVES:

- tounderstandthefundamentalsofDSP
- tolearnvariousDSPstructuresandtheirimplementation.
- toknowdesigningconstraintsofvariousfilters
- designandoptimizeVLSIarchitecturesforbasicDSPalgorithms
- toenablestudentstodesignVLSIsystemwithhighspeedandlowpower.
-

UNITI INTRODUCTIONTODIGITALSIGNAL PROCESSING 9

Linearsystemtheory-convolution-correlation-DFT-FFT-basicconceptsinFIRfiltersandIIR filters- filter realizations. Representations of DSP algorithms- block diagram-SFG-DFG.

UNITII ITERATIONBOUND,PIPELININGANDPARALLELPROCESSING OF FIR FILTER 9

Data-flowgraphrepresentations-LoopboundandIterationboundalgorithmsforcomputingiteration bound-LPM algorithm. Pipelining and parallel processing: pipelining of FIR digital filters- parallel processing, pipelining and parallel processing for low power, Computational complexity.

UNITIII RETIMING,UNFOLDINGANDFOLDING 9

Retiming: definitions, properties and problems- solving systems of inequalities. Properties of Unfolding, critical path, Unfolding and Retiming, applications ofUnfolding, Folding transformation- register minimization techniques, register minimization in folded architecture- folding of multiratesystem.

UNITIV FASTCONVOLUTION 9

Cook-toomalgorithm-modifiedcook-Toomalgorithm.Designoffastconvolutionalgorithmby inspection - Winograd algorithm- modified Winograd algorithm

UNITV ARITHMETICSTRENGTHREDUCTION INFILTERS 9

ParallelFIRfilters-fastFIRalgorithms-twoparallelandthreeparallel.Parallelarchitecturesforrank orderfilters-odd-even,merge-sortarchitecture-rankorderfilterarchitecture-parallelrankorder filters-runningordermergeordersorter,lowpowerrankorderfilter.

TOTAL:45 PERIODS

PRACTICAL EXCERCISES

Simulations using Verilog/MATLAB/Python

1. Design and Implementation of FIR and IIR Filter Architectures
2. Design and Implementation of FFT Processor Architecture
3. Implementation of Pipelining and Parallel Processing Techniques for FIR Filters
4. Implementation of Retiming and Folding Transformations for DSP Architectures

5. Design and Implementation of Fast Convolution using Winograd/Cook-Toom Algorithms

REFERENCES

1. K.KParhi:“VLSIDigitalSignalProcessing”,John-Wiley,2ndEditionReprint,2018.
2. 2.John G.Proakis, Dimitris G.Manolakis, “Digital SignalProcessing”,Prentice Hall ofIndia,1st Edition, 2015.

23VDP064 BIOSIGNALPROCESSING LTPC
3024

COURSEOBJECTIVES:

Thestudentshouldbemadeto:

- Tostudythecharacteristicsofdifferentbiosignals
- Tolearnlinearandnon-linearfilteringtechniquestoextract desiredinformation
- Tounderstandvarioustechniquesforautomatedclassificationanddecisionmakingtoaid diagnosis

UNITI BIOSIGNALANDSPECTRALCHARACTERISTICS 9

Characteristics of some dynamic biomedical signals, Noises- random, structured and physiological noises.Filters-IIRandFIRfilters.Spectrum–powerspectraldensityfunction,cross-spectraldensity and coherence function, cepstrum and homomorphic filtering. Estimation of mean of finite time signals.

UNITII TIMESERIESANALYSISANDSPECTRALESTIMATION 9

Timeseriesanalysis-linearpredictionmodels,processorderestimation,latticerepresentation,non-stationary process, fixed segmentation, adaptive segmentation, application in EEG, PCG signals, Time varyinganalysisof Heart-ratevariability,modelbasedECGsimulator.Spectralestimation – Blackman Tukey method, periodogram, and model based estimation. Application in Heart rate variability, PCG signals.

UNITIII ADAPTIVEFILTERINGANDWAVELETDETECTION 9

Filtering-LMS adaptivefilter,adaptivenoise canceling inECG, improvedadaptivefiltering inECG, Wavelet detection in ECG – structural features, matched filtering, adaptive wavelet detection, detection of overlapping wavelets.

UNITIV BIOSIGNALCLASSIFICATIONANDRECOGNITION 9

Signalclassificationand recognition – Statistical signalclassification, lineardiscriminantfunction, direct feature selection and ordering, Back propagation neural network based classification. Application in Normal versus Ectopic ECG beats.

UNITV TIMEFREQUENCYANDMULTIVARIATEANALYSIS 9

Time frequency representation, spectrogram, Wigner distribution, Time-scale representation, scalogram, wavelet analysis – Data reduction techniques, ECG data compression, ECG characterization, Feature extraction- Wavelet packets, Multivariate component analysis-PCA,ICA.

PRACTICAL EXERCISES:

Simulations using Python/MATLAB or Equivalent Open-Source Tools

1. Design and Implementation of FIR/IIR Filters for Biosignal Denoising
2. Implementation of Time Series Analysis and Spectral Estimation for ECG/EEG Signals
3. Implementation of Adaptive Filtering and Wavelet-Based ECG Feature Detection
4. Implementation of Statistical and Neural Network-Based Biosignal Classification
5. Implementation of Feature Extraction using Wavelet Transform and Principal Component Analysis (PCA)

COURSEOUTCOMES:

Onsuccessfulcompletionofthiscourse,thestudentwillbeableto

CO1:PreprocesstheBiosignals.

CO2:Analyzebiosignalsintimedomain&toestimatethespectrum.CO3:Applywaveletdetection techniques for biosignal processing.

CO4:ClassifyBiosignalsusingneuralnetworksandstatisticalclassifiers.CO5:Extractthefeatures using multivariate component analysis.

TOTAL:45PERIODS

TEXTBOOKS

1. RangarajM.Rangayyan,"BiomedicalSignalAnalysis-Acasestudyapproach", Wiley, 2nd Edition, 2016.
2. WillisJ.Tompkins,"BiomedicalDigitalSignalProcessing",PrenticeHallofIndia, New Delhi, 2003.
3. ArnonCohen,"Bio-MedicalSignalProcessingVolIandVolII",CRCPressInc., Boca Rato, Florida, 1999.

REFERENCES

1. KayvanNajarianandRobertSplerstor,"BiomedicalsignalsandImage processing'',CRC-TaylorandFrancis,NewYork,2nd Edition,2015.
2. K.P.Soman,K.Ramachandran,"Insightintowaveletfromtheorytopractice",PHI, New Delhi, 3rd Edition, 2015.
3. D.C.Reddy,"BiomedicalSignalProcessing-PrinciplesandTechniques'',Tata McGraw-Hill Publishing Co. Ltd, 2015.
4. JohnL.Semmlow,"BiosignalandBiomedicalImageProcessingMatlabBased applications'', Taylor& Francis Inc, 2015.

23VDP065 DIGITALIMAGEANDVIDEOPROCESSING L TPC 3024

COURSEOBJECTIVES:

- Toprovidethestudentwithbasicunderstandingofimagefundamentalsandtransforms
- Toprovideexposuretothestudentsaboutimageenhancementandrestoration
- Toimpartathoroughunderstandingaboutsegmentationand Recognition.
- ToknowtheVideoProcessingandmotionestimation
- Learningtheconceptswillenablestudentstodesignanddevelopanimageprocessing application .

UNITI FUNDAMENTALSOFIMAGEPROCESSINGANDTRANSFORMS 9

Introduction, Image sampling, Quantization, Resolution, Image file formats, Elements of image processing system, Need for transform, image transforms, Fourier transform, 2 D Discrete Fourier transform ,Walsh transform, Hadamard transform, Haar transform, KL transform, singular value decomposition, Radontransform, comparisonofdifferent imagetransforms. Digital Cameraworking principle.

UNITII ENHANCEMENTANDRESTORATION 9

Spatialdomainmethods:Histogramprocessing,FundamentalsofSpatialfiltering,Smoothing spatialfilters,Sharpeningspatialfilters.Frequencydomainmethods:Basicsoffilteringinfrequency domain,imagesmoothing,imagesharpening,IntroductiontoImagerestoration,Imagedegradation, Imagerestorationmodel,LinearandNonlinearimagerestorationtechniques,Blinddeconvolution. Color image enhancement.

UNITIII SEGMENTATIONANDRECOGNITION 9

Edgedetection,EdgelinkingviaHoughtransform–Thresholding–Regionbasedsegmentation– Regiongrowing–Regionsplittingandmerging–Morphologicalprocessing-erosionanddilation, Boundary representation, Boundary description, Fourier Descriptor, Regional Descriptors – Topological feature, Texture – Patterns and Pattern classes – Recognition based on matching.

UNITIV BASICSTEPSOFVIDEOPROCESSING 9

Analog Video, Digital Video. Time-Varying Image Formation models:Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation,Sampling of Videosignals, Filtering operations

UNITV 2-DMOTIONESTIMATION 9

Opticalflow, opticalflow constraints, GeneralMethodologies, PixelBased MotionEstimation, Block-Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation,Multiresolutionmotionestimation,Waveformbasedcoding,Blockbased transformcoding,Predictive coding,Applicationofmotionestimation inVideocoding.

45PERIODS

PRACTICALEXERCISES: **15 PERIODS**

1. HistogramEqualization
2. ImageFiltering(spatial-domain)
3. ImageFiltering(frequency-domain)
4. ImageSegmentation
5. FamiliarizationwithVideoProcessingtools
6. Denoisingvideo
7. Videoresizing
8. Background subtraction
9. Interpolationmethodsforre-sampling
10. Adaptiveunsharpmaskingbasedinterpolationforvideoup-sampling
11. Gaussianmixturemodel(GMM)basedbackgroundsubtraction
12. Videoencoding

COURSEOUTCOMES:

Onthesuccessfulcompletionofthecourse,studentswillbeableto

CO1: Analyzethedigitalimage,representationofdigitalimageanddigitalimagesintransform Domain.

CO2: Analyzethedetectionofpoint,lineandedgesinimagesandunderstandtheredundancyin images, various image compression techniques.

CO3:Analyzethevideotechnologyfromanalogcolor TVsystemstodigitalvideosystems,how videosignalissampledandfilteringoperationsinvideoprocessing.

CO4: Obtainknowledgeingeneralmethodologiesfor2Dmotionestimation,variouscodingusedin video processing.

CO5: Designimageandvideoprocessingsystems.

TOTAL:60PERIODS

REFERENCES:

1. DigitalImageProcessing-GonzalezandWoods,3rdEd.,Pearson, 2020
2. HandbookofImageandVideoprocessing,Academicpress,2015
3. AnilKumarJain,FundamentalsofDigitalImageProcessing,PrenticeHallofIndia.2ndedition, 2015
4. RCGonzalez,REWoodsandSLEddins,DigitalImageProcessingUsingMatlab,Pearson Education , 2020.